DESIGN AND DEVELOPMENT OF HIGH FREQUENCY HIGH EFFICIENCY MULTIPLE OUTPUTS FORWARD CONVERTER BASED ON UCC2891

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ABSTRACT

This paper presents high frequency high efficiency multiple outputs DC-DC converter. Proposed converter is designed using forward converter topology followed by active clamp reset; using UCC2891 as a PWM controller. For meeting the high operating frequency, high efficiency requirement active reset topology is considered for the forward converter as it provides optimum transformer rest with benefits of recycling the transformer leakage energy while minimizing the voltage stress across the main switch. Optocoupler is used for isolation in the control loop, as it gives proper isolation with minimized circuit complexity and cost reduction. This paper provides the detail design and development of high frequency high efficiency 50W active clamp forward converter with multiple outputs.

Keywords: Active Clamp, Forward Converter, ZVS.

I. INTRODUCTION

Forward converter has been mainly popular choice for medium power application in DC-DC power conversion. The main concern in forward converter is the resetting of the transformer. So far there has been various reset mechanism known such as third winding, RCD, resonant type in order to avoid the transformer saturation. However, the lower efficiency, complicated transformer winding structure and the cost of too many added elements are the main drawbacks of these core reset methods. Active clamp mechanism is the newest and most efficient transformer reset mechanism known today [1]. But the disadvantages associated with active clamp are complex Gate Drive circuitry, advanced PWM control technique requirement, etc. With Texas Instruments incorporated and its subsidiaries (TI) introduced a new generation of active clamp controller, UCC2891; which has features that covers all the disadvantaged associated with active clamp topology.
A detailed design and implementation of high frequency multiple outputs forward converter with UCC2891 active clamp PWM controller is explained in this paper.

II. DESIGN SPECIFICATION

This converter is designed for the following specifications:

- Input voltage range = 16V to 50V
- Switching frequency = 400Khz
- Efficiency = 85%
- \( D_{MAX} = 0.50 \)
- \( D_{MIN} = 0.16 \)
- The output voltage and load current are:
  
<table>
<thead>
<tr>
<th>Output 1</th>
<th>5V/4A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output 2</td>
<td>+15V/1A</td>
</tr>
<tr>
<td>Output 3</td>
<td>-15V/1A</td>
</tr>
</tbody>
</table>

- Total output power = 50W

Features:

- Active clamp reset method (using UCC2891)
- High operating frequency
- Main output isolated from dual outputs
- Under voltage lockout
- Short circuit protection

This converter is designed using **Single Ended Forward Converter Topology** followed by Coupled Inductor and LDOs (Low drop out regulators) for slave outputs to meet the required specifications. The block schematic of the converter is shown in fig. 1.
III. DESIGN PROCEDURE

For any power supply design, the success of meeting a set of given design specification starts with a careful designed power stage, control loop and finally setting up the PWM controller [2-3].

Abbreviations:
- \( V_{IN\,(MIN)} \): minimum input voltage
- \( V_{IN\,(MAX)} \): maximum input voltage
- \( V_{ON} \): input turn-on voltage
- \( V_{OFF} \): input turn-off voltage
- \( V_{OUT} \): output voltage
- \( P_{OUT} \): output power
- \( V_D \): diode drop
- \( \eta \): efficiency
- \( F_{SW} \): Switching frequency
- \( T_S \): switching period
- \( D_{MAX} \): max duty cycle
- \( D_{MIN} \): minimum duty cycle
- \( N_P \): primary no of turns of transformer
- \( N_S \): secondary no. of turns of transformer
- \( A_P \): area product of the core
- \( A_C \): cross-sectional area of the selected core
- \( K_W \): window factor:0.4
- \( J \): current density
- \( B_m \): flux density
- \( E \): energy stored in the inductor
- \( L_P \): primary inductance of the coupled inductor

A. Transformer Design

Transformer is designed by calculating the area product \( A_P \) and by selecting the suitable core by using the following formula.

\[
A_P = \sqrt{\frac{P_{OUT}}{F_{SW}} \cdot \frac{(1 + \frac{1}{\eta})}{K_W \cdot J \cdot 10^{-6} B_m \cdot F_{SW}}} \quad (1)
\]

The transformer core that has area product more than the calculated value is selected.

Selected POT core part number is OR41811UG.

Primary number of turns \( (N_P) \) is given as

\[
N_P = \frac{V_{IN\,(MIN)}}{B_m \cdot A_C \cdot 10^{-6} \cdot F_{SW}} \cdot \frac{D_{MAX}}{B_m \cdot A_C \cdot 10^{-6} \cdot F_{SW}} \quad (2)
\]

Turns ratio can be calculated as

\[
T_{ratio} = \frac{N_S}{N_P} \cdot \frac{(V_{IN\,(MIN)} + V_D) + V_D \cdot D_{MAX}}{D_{MAX\cdot} V_{IN\,(MIN)}} \quad (3)
\]
B. Active Clamp Reset

![Block diagram of the active clamp forward converter](image)

**Fig. 2** Block diagram of the active clamp forward converter

In the fig 2, the forward transformer has been replaced with equivalent circuit model showing the magnetizing, Lm and leakage inductances Lr (represents the sum of transformer leakage inductance and external inductance). The auxiliary switch Q2 and clamp capacitor Cc represent the active clamp circuit [4].

The basic concept of active clamp mechanism is that during the turn off of the main switch, a capacitor, with a voltage greater than \( V_{\text{IN}} \), can be used to apply a reversed voltage across the primary of the transformer. The reversed voltage will force the magnetizing current to reverse slope and reset the magnetizing current. An auxiliary switch is necessary to disconnect the capacitor while the main switch is active. Thus after each switching duty cycle, the magnetizing current in the power transformer is reset hence preventing core saturation.

![Waveforms of the Gate (V_{GS}), magnetizing current (i_{LM}) and voltage across main mosfet (V_{DS}) of the forward converter](image)

**Fig. 3** Waveforms of the Gate (\( V_{GS} \)), magnetizing current (\( i_{LM} \)) and voltage across main mosfet (\( V_{DS} \)) of the forward converter

Fig. 3 show the drain-to-source voltage, \( V_{DS} \), of the main power MOSFET switch. During the turn on time, when the gate pulse \( V_{GS} \) of the main switch, Q1 is given, the magnetizing current is ramp up linearly. During the turn off time of Q1, the gate pulse of the auxiliary switch is given, turning on the switch Q2. As Q2 is turn on clamp capacitor, \( C_{CL} \) voltage plus \( V_{\text{IN}} \) (\( V_{\text{IN}}+V_{\text{CL}} \)) is applied across the magnetizing inductance with reversed polarity. The slope of the magnetizing current is going to change from a positive one to a negative one as shown in the above figure; the magnetizing current is reset to its initial value.
Advantages of active clamp reset topology:
- "Recycles" transformer magnetizing energy.
- Facilitates zero voltage transition of the main switch for higher efficiency.
- Operates at fixed frequency.

The voltage stress of the main switch Q1 is given as sum of $V_{\text{CL}}$ (clamp voltage) and $V_{\text{IN}}$

$$V_{Q1} = V_{\text{CL}} + V_{\text{IN}} \quad (4)$$

In the steady state, the voltage-second product when main switch or body diode is turned on equals the voltage-second product when both main switch and body diode are turned off. One can obtain the clamp capacitor voltage is given as:

$$V_{\text{CL}} = \frac{D V_{\text{IN}}}{1 - D} \quad (5)$$

Selecting Clamp Capacitor:
The clamp capacitor value is solved such that the resonant time constant is much greater than the maximum off-time:

$$2 \times \pi \times \sqrt{L_{\text{mag}} \times C_{\text{CL}}} = t_{\text{off(max)}} \quad (6)$$

Multiplying above equation by a factor of 10 to assure that the inequality of holds true and expressing $C_{\text{CL}}$ in terms of known design parameters:

$$C_{\text{CL}} > 10 \times \frac{(1 - D_{\text{min}})^2}{L_{\text{mag}} \times (2 \pi \times F_{\text{sw}})^2} \quad (7)$$

C. Switching MOSFET Selection
Selected MOSFET: IPP200N15N3 G, 150V, 50A, $R_{DS}$: 20mΩ, TO-220.

D. Output Filter
Capacitance value with respect to load transient from No load to 100% load:

$$C_{\text{L}} = \frac{E_{\text{IN}}}{\Delta V_{\text{OUT}}} \quad (8)$$

Coupled inductor primary inductance:

$$L_p = \frac{[(E_{\text{OUT}} + E_p)(1 - D_{\text{MIN}})T_p]}{\Delta I} \quad (9)$$

The selection of the core can be done by calculating the area product.

$$A_p = \frac{12 \times E_p}{B_p \times K_p \times f \times m^4} \quad (10)$$

Calculate the number of turns given by the equation

$$N = \frac{L_p \times I_{FR}}{A_{\text{CL}} \times B_{\text{pH}}} \quad (11)$$
Calculate turns for the coupled inductor

\[ A_L = \frac{L_2}{A_L} \]  \hspace{1cm} (12)

\[ A_L = \sqrt{\frac{L_2}{A_L}} \]  \hspace{1cm} (13)

E. Active clamp PWM controller UCC2891

The disadvantages associated with active clamp are the need for precise duty clamp and the need for advanced control technique to synchronize delay timing between the active clamp and main switch gate drive. UCC2891 provides features such as the programmable maximum duty cycle clamp accurate to within ±3 percent, a programmable delay time between the main switch and clamp switch. Hence the disadvantages associated with using active clamp technique are nonexistent when UCC2891 is used as the control IC.

The delay time between the turn off of Q2 and the turn on of Q1 is critical to ZVS operation of the main switch. The optimum value of the resonant period formed by \( L_r \) and \( C_{OSS} \):

\[ T_{delay} = \frac{\pi}{2} \sqrt{L_r C_{OSS}} \]  \hspace{1cm} (14)

Fig. 4 UCC2891 set up diagram
The required turn-on delay (T_{\text{DELAY}}) of the gate drive signals is defined in eqn. (15). The corresponding R_{\text{DEL}} resistor value to implement this delay is given by:

\[ R_{\text{DEL}} = (T_{\text{DELAY}} - 50 \times 10^{-12}) \times 0.87 \times 10^{-14} \]  

(15)

The oscillator frequency and maximum duty cycle clamp are set by R_{\text{ON}} and R_{\text{OFF}} according to the following eqns.

\[ R_{\text{ON}} = \frac{T_{\text{ON}}}{97.33 \times 10^{-12}} = \frac{D_{\text{MAX}}}{T_{\text{UV}} \times 97.33 \times 10^{-12}} \]  

(16)

\[ R_{\text{OFF}} = \frac{T_{\text{OFF}}}{18 \times 10^{-11}} = \frac{1 - D_{\text{MAX}}}{T_{\text{UV}} \times 18 \times 10^{-11}} \]  

(17)

F. Under voltage lockout

UCC2891 also features accurate line UV lockout. When the circuit initially starts, a rising input on LINEUV enables the outputs when the threshold of 1.27 V is crossed. The under voltage threshold is set by setting the value of R_{\text{IN1}} and R_{\text{IN2}} as follows.

The amount of hysteresis current fed back to the LINEUV comparator is first calculated.

\[ I_{\text{HYST}} = \frac{2.5}{R_{\text{UV2}}} \times 0.08 \]  

(18)

\[ R_{\text{UV2}} = \frac{V_{\text{ON}} - V_{\text{OFF}}}{I_{\text{HYST}}} \]  

(19)

\[ R_{\text{IN2}} = R_{\text{UV2}} \times \frac{1.27}{V_{\text{OFF}} - 1.27} \]  

(20)

where, \( V_{\text{ON}} = [V_{\text{IN (MIN)}} - 1] \) and \( V_{\text{OFF}} = [V_{\text{IN (MIN)}} - 2] \).

IV. DESIGN CHALLENGES

A. LDO design

A low drop out regulator is used to maintain steady voltage at terminals 2 and 3.

![Fig.5 Low Drop-Out regulator circuit](image-url)
The main components are a MOSFET and a differential amplifier (error amplifier, Q1 and Q2). One input of the differential amplifier monitors the fraction of the output determined by the resistor ratio of R4 and R5. The second input to the differential amplifier is from a stable voltage reference (2.5V reference). If the output voltage rises too high relative to the reference voltage, the drive to the power FET changes to maintain a constant output voltage.

For the circuit given in the fig. 5 the output voltage is given as

$$v_{out} = \left(1 + \frac{R_4}{R_5}\right) v_{ref} \quad (21)$$

**Fig. 6** Short circuit protection circuit

**B. Short Circuit Protection**

Primary side current sensing is done using a current sense transformer. The sense current is given to the input of Opamp U1 (LM158) through resistor R3, where it is amplified by the amplifier U1A, and then the output is given to comparator U1B, where the input is compared with the reference voltage, fixed at 2.5V by the two resistors R8 and R9. Once the input voltage to U1B goes beyond 2.5V the zener diode is forward biased, which activates the shutdown function of the PWM controller.

**V. CIRCUIT SCHEMATIC AND TEST RESULTS**

**A.** The circuit schematic of the prototype 50W active clamp forward converter based on UCC2891 is shown in fig. 7.
50 WATTS CURRENT MODE, ACTIVE CLAMP FORWARD CONVERTER: Fsw: 400 KHz

Fig. 7 Active clamped forward converter circuit schematic
B. The test readings of the experimental prototype are shown in Table I, Table II.

### Table I. Test data with efficiency calculation

<table>
<thead>
<tr>
<th>$V_{IN}$ (V)</th>
<th>$I_{IN}$ (A)</th>
<th>$V_{O1}$ (V)</th>
<th>$V_{O2}$ (V)</th>
<th>$V_{O3}$ (V)</th>
<th>$\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>3.9</td>
<td>5.0020</td>
<td>14.90</td>
<td>-14.92</td>
<td>80.13</td>
</tr>
<tr>
<td>36</td>
<td>1.76</td>
<td>5.0018</td>
<td>14.87</td>
<td>-14.90</td>
<td>78.91</td>
</tr>
<tr>
<td>50</td>
<td>1.3</td>
<td>5.0015</td>
<td>14.85</td>
<td>-14.88</td>
<td>77</td>
</tr>
</tbody>
</table>

### Table II. Test data (line regulation reading)

<table>
<thead>
<tr>
<th>Load</th>
<th>$V_{O1}$:5V/4A</th>
<th>$V_{O2}$:+15V/1A</th>
<th>$V_{O3}$:-15V/1A</th>
</tr>
</thead>
<tbody>
<tr>
<td>10%</td>
<td>0.07</td>
<td>0.0139</td>
<td>0.0144</td>
</tr>
<tr>
<td>50%</td>
<td>0.013</td>
<td>0.0256</td>
<td>0.0265</td>
</tr>
<tr>
<td>100%</td>
<td>0.014</td>
<td>0.053</td>
<td>0.0588</td>
</tr>
</tbody>
</table>

VI. WAVEFORMS

The waveforms of the experimental prototype are shown in fig.6, fig. 7, fig. 8 and fig. 9.

![Fig. 6 Main mosfet gate pulse at 16V (input voltage)](image1)

![Fig. 7 Main mosfet drain waveform at 16V (input voltage)](image2)
VI. CONCLUSION

A high frequency high efficiency multiple outputs 50W forward converter with active clamp PWM controller UCC2891 is been presented with experimental results and key waveforms in this paper. The complexity associated with active clamp topology is greatly simplified with the used of UCC2891 as the PWM controller IC. With active clamp topology, various advantages over other reset mechanism could be achieved. Such as optimum transformer core reset, fixed frequency operation, high efficiency, etc. The prototype was developed in a general purpose board and still efficiency up to 80% has been achieved. Hence we can expect efficiency more than 90% for the same systems develop in PCB with proper rooting.

REFERENCES