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RELIABILITY MEASUREMENT OF MEMORY SYSTEM USING SPARE BLOCKS

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ABSTRACT

Reliability requirements depend on the application. Missile and space borne application require high levels of reliability whereas ground based applications require lower levels of reliability. The reliability of these systems can be achieved by using redundancy and repair. Reconfiguration (repair) of memory arrays with the help of spare memory lines is the most used technique for reliability improvement of memories with faults. Faulty cell in memory arrays are closely spaced.. This is called as fault clustering. This paper initially examines a quadrat-based fault Model for memory elements under clustered faults to define a foundation of measurement. Then reliability calculations are done long-life dependability of a fault-tolerant memory system with hierarchical active redundancy, which consists of spare columns in each memory module.

Key words: Onboard memory systems, Memory reconfiguration (repair), Hierarchical active redundancy, Clustered faults, Quadrat-based fault model, Reliability

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1. INTRODUCTION

According to the Semiconductor Industry Association (SIA) and ITRS 2001, the comparative silicon area occupied by memories in embedded systems will approach 94% by 2017 [1-4]. For example, the Compaq Alpha EV7 chip uses 135 million transistors for RAM cores alone, while the entire chip has 152 million transistors. Since embedded memories have higher density and complexity than other digital blocks, they have higher failure probabilities. Therefore, suitable fault-tolerant technique should be incorporated into the chip at the design stage. In general, the performance and manufacturing yield of embedded memories can be improved by the incorporation of redundancy. The usual methods to add redundancy into an embedded memory array include the following.

- **Redundant rows or redundant columns** [5], [6]: By using this approach, spare rows or columns are built into the memory array. One of these spare rows/columns is used to replace the faulty column. The advantage of this one-dimensional approach is that it can be implemented easily. The repair efficiency of this method can be low since a faulty row (column) cannot be replaced by the redundant columns (rows).
- **Redundant rows and redundant columns** [5]–[8]: In this approach, both redundant rows and columns are part of the memory array. When a faulty cell is detected, a redundant row or a redundant column to replace it. It is more efficient than the first approach when more faulty cells exist in the memory array. The main defect of this approach is that the optimal redundancy allocation problem becomes NP-complete [9-13]. Although many heuristic algorithms have been proposed to solve this problem, it is still difficult to develop on-chip implementations for these algorithms. Due to high data rates of today's system-on-chip (SOC) designs, we usually have long bit lines and word lines for embedded memories. The objective of this paper is to clearly measure the dependability of a fault-tolerant memory system using fault clustering, and aiming at accurate prediction of reliability (i.e., the conditional probability that the system performs satisfactorily throughout a time interval) and mean-time-to failure (MTTF, i.e., the expected time that a system will operate before it fails). This facilitates the design of reliable mission-specific onboard memory systems while maintaining minimal redundancy. To properly model the faulty memory arrays, a accurate fault model must be defined. It is well known that faults in VLSI circuits tend to occur in groups due to defects that span multiple circuit elements [4], [5], [11], [13]. This physical property is referred to as defect clustering. Poisson distributions [4], [5], [14-18] are to deal with defect clustering. In these models, the wafer is divided into multiple regions and in the each region; the defects are modeled as Poisson. Models that use compounded distributions are quadrat - based because they assume different distributions in different regions (quadrats) of the wafer. For quadrat-based models, defects occur s-dependently in the same quadrat, while occurrences of defects in different quadrats are s-independent [4]. Another approach to modeling defects is the center-satellite approaches [11] wherein there are separate distributions are used for the locations of cluster centres. The resulting models using center-satellite approach have more parameters: making the problem of parameter estimation more complex. Then quadrat-based models [4] are simple and easy to make calculations. The quadrat-based model makes it possible to accurately measure the reliability of memory arrays with clustered faults.

The objective of this paper is to thoroughly measure the dependability of a fault-tolerant memory systems under fault clustering, and achieving more accurate prediction of reliability (i.e., the conditional probability that the system performs correctly throughout a time interval) and mean-time-to failure (MTTF, i.e., the expected time that a system will operate before it fails). Thereby, allowing selection of memory systems in terms of reliability and MTTF while maintaining minimal redundancy for various ground or space applications.

The organization of this paper is as follows: In the next section, review and preliminaries related to this research work will be given. In Section III, a fault-tolerant memory system with active redundancy proposed in [9] is reviewed. Non Fault tolerant reliability measurements and fault-tolerant memory modules with a clustered fault model are discussed in Sections IV and V, respectively. Parametric simulation and its results are given in section VI. Conclusions and Discussions are elaborated in the final section.

2. INTRODUCTION AND FUNDAMENTALS OF CLUSTERED FAULT MODEL

The following notation is used in this paper:

n : number of rows and columns in an array, excluding spares.

A_n : a n x n memory array with n rows and n columns.

$a_{i,j}$: an element of $\boldsymbol{A_n}$

s : number of spare columns.

m_n : number of rows and columns in a quadrat.

$\eta = n / m_n$.

p_1 : Pr{a quadrat is FP} (see below).

p_2: fault arrival rate of a memory cell within FP quadrat.

P_3 : fault arrival rate of a memory cell within FR quadrat (see below).

λ: parameter of a Poisson random variable.

t : time.

R : reliability, the conditional probability that the system performs correctly throughout Δt.

The following assumptions are made in this paper:

- Quadrats are of two types: Fault Prone Quadrat (denoted by FP) and Fault Resistant Quadrat (denoted by FR). FPs are susceptible to faults while FRs resists faults.
- Within any quadrat, faults occur s-independently.
- A quadrat is FP with probability p_1, s-independently of other quadrats.
- Occurrence of faults in FP quadrats is determined by p_2.
- Occurrence of faults in FR quadrats is determined by p_3.
- P2>>p3 & p3=0(approx).
- $\overline{p1}$>>p1 & η.p1<=1.
- η is an integer.

To improve the reliability of embedded memories, Fault tolerance techniques are used by incorporating spare rows and spare columns. But this increases area overhead. With more area overhead the cost also increases. So the area overhead is to be minimized [1], [2], [4], [5], [12]. .Thus, an appropriate optimization of acceptable reliability and redundancy area is desirable for high reliability, low-cost manufacturing of memory arrays.

In this paper, an n x n memory array, A_n, is divided into quadrats consisting of m_n x m_n cells. Above mentioned assumptions rule the occurrence of faults within such an array. Assumption (1) defines what is required for a quadrat to be FP or FR: the arrays are classified into 'quadrats with a high density of faulty cells' and 'quadrats with a low density of faulty cells'. The probability of a cell being faulty is p1 • p2 + $\overline{p1}$ • p3. However, if some of the neighbors of a cell are faulty, the probability of that cell's being faulty increases towards p2 since it is more likely that the cell lies in a FP quadrat. Figure (1) illustrates the effect of the Clustered-Fault model. Figure (la) uses the quadrat-based fault model with n = 16, m_n= 4, p1=0.11, p2= 0.52 and p3 = 0.021 for the faulty memory array. Figure (1b) uses a random fault model with failure-probability = 0.067.

A faulty column (row) containing more than one faulty cell is referred to as Connective Faulty Column (CFC) (CFR) [6]. 7 CFC s are available in the memory array in Figure (la) whereas 13 CFC s are available in the memory array in Figure (lb). Figure 2 shows the repair of cells using spare columns. Figure (2a) shows the reconfiguration using 8 spare lines while Figure (2b) shows the reconfiguration using 14 spare lines.

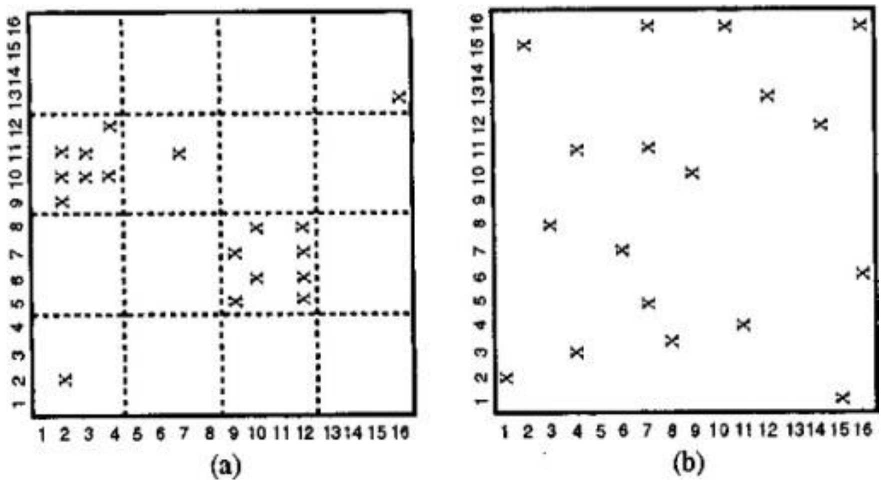

Figure 1 Faulty Memory Arrays generated with: a. Clustered-Fault Model b. Random-Fault Model

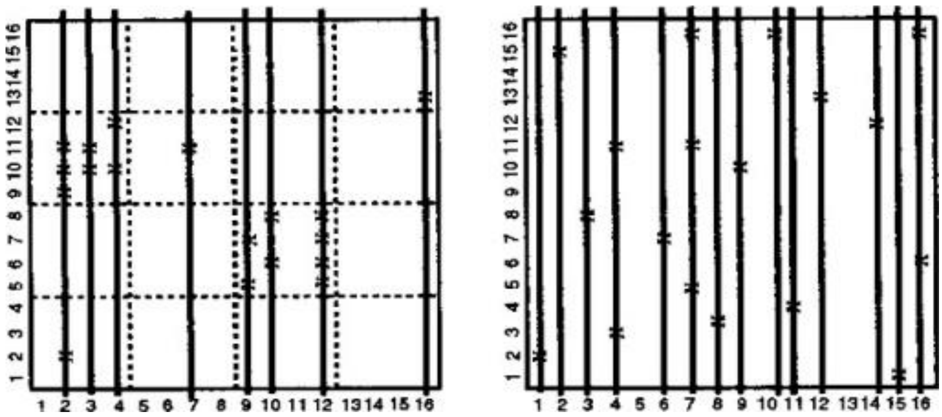

Figure 2 Repaired Fault Arrays generated with: a. Clustered-Fault Model b. Random-Fault Model

The average number of faulty cells covered per spare line is referred to as covering ratio. For example, covering ratio of the reconfiguration given in Figure (2a) is 2.2514 whereas covering ratio of the reconfiguration given in Figure (2b) is 1.28. It is quite intuitive that less number of spare lines would be required to repair a given memory array if faulty cells closely spaced (i.e., fault clustering).

3. RELIABLITY MEASUREMENT OF NON-FAULT-TOLERANT MEMORY MODULE WITH CLUSTERED FAULT MODELS

Let us consider a memory module A_n of n x n dimensions. For example, memory module shown in Figure (1) can be visualized as n = 16, m_n = 4 and η= 4. A quadrat is FP with probability p1, s-independently of other quadrats. Pr{quadrat is FR} = $\overline{p1}$ Pr{quadrat is FP) = p1. Fault occuring rate in a FP quadrat is $\lambda FP = p2 \bullet m_n^2$ and fault occurring rate in a FR quadrat is $\lambda_{FR} = p3 \bullet m_n^2$ Then, reliability of FP is calculated by the exponential failure law $R_{FP}(t) = e^{-\lambda_{FP} t}$ and reliability of FR is $R_{FR}(t) = e^{-\lambda_{FR} t}$. As Pr{quadrat is FP} = p1 and Pr{quadrat is

FR} $=\overline{p1}$, expected number of FP quadrats in a quadrat-column is p1.η and expected number of FR quadrats in a quadrat-column is $\overline{p1}$.η. So, reliability of a quadrat-column is

$$R_{QC}(t) = (p1\ e^{-\lambda Fpt} + \overline{p1}\ e^{-\lambda Frt})^{\eta} \qquad (1)$$

Finally, overall reliability of a non-fault-tolerant memory module an becomes

$$R_{NFTAn}(t) = (R_{QC})^{\eta} \qquad (2)$$

4. RELIABILITY MEASUREMENT OF FAULT-TOLERANT MEMORY MODULE WITH CLUSTERED FAULT MODEL

The given memory array A_n consists of approximately $\eta^2 \bullet p1$ FP quadrats and $\eta^2 \bullet \overline{p1}$ FR quadrats. For each FP quadrat, P_r{a column in FP quadrat is faulty} = 1 - P_r{a column in FP quadrat is fault-free} is

$$1 - (1 - P_2)^{m_n} \qquad (3)$$

Furthermore, the expected number of faulty columns in a FP quadrat becomes

$$m_n \bullet (1 - (1 - P2)^{m_n}) \qquad (4)$$

Since P2 >>P3, η.p1<=1, and P3=0(approx), the FR quadrats are essentially fault-free and the FP quadrats primarily dictate the locations of the faulty cells. So the expected number of faulty columns in a quadrat-column is primarily determined by the faulty columns in FP quadrats. Thus, the expected number of faulty columns in a quadrat-column is

$$\lambda_{QC} = m_n \bullet (l - (1 - P2)^{m_n \cdot \eta \cdot p1} \qquad (5)$$

And the overall expected number of faulty columns in a memory module An becomes

$$\lambda_{An} = .\lambda_{QC} \bullet \eta \qquad (6)$$

So, the failure rate of a single column can be estimated as

$$\lambda_{col} = \lambda A_n / \eta \qquad (7)$$

and the reliability of a single column can be expressed as

$$Rcol(t) = e^{-\lambda colt} \qquad (8)$$

Every memory module contains of n columns and s spare columns and minimum of n out of the total of n + s columns are required to work for the memory module to function. Thus, the reliability of the fault-tolerant memory module with s spare columns can be written as

$$R_{FTAn}(t)$$

$$= \sum_{i=0}^{s} \binom{n+s}{i} R_{\mathrm{col}}(t)^{n+s-i} \cdot \overline{R_{\mathrm{col}}(t)}^{i} \qquad (9)$$

$$\approx e^{-\lambda A_n (n+s)} \cdot \sum_{i=0}^{s} (\lambda_{A_n}(n+s))^i / i! \qquad (10)$$

5. PARAMETRIC SIMULATION

The reliability of the fault-tolerant memory system using fault clustering is studied through numerical experiments in this section. Parameters used in this simulation are summarized in Table I. The unit time interval is a week.

In Figure (3), the reliability of 128 X 128 memory module for different spare columns is depicted whereas In Figure (4), the reliability of 256X256 memory module for different spare columns is is shown. Summary of assumed parameters are shown in Table I.

Table 1 Summary of simulation parameters

For 128 X 128 Memory Module

Parameter	n	n2	η^2	$(m_{n})^2$	s	P1	p2
Value	128	16K	32	512	variable	5×10^{-4}	5×10^{-3}

For 256 X 256 Memory Module

Parameter	n	n2	η^2	$(m_{n})^2$	s	P1	p2
Value	256	64K	64	1024	variable	5×10^{-4}	5×10^{-3}

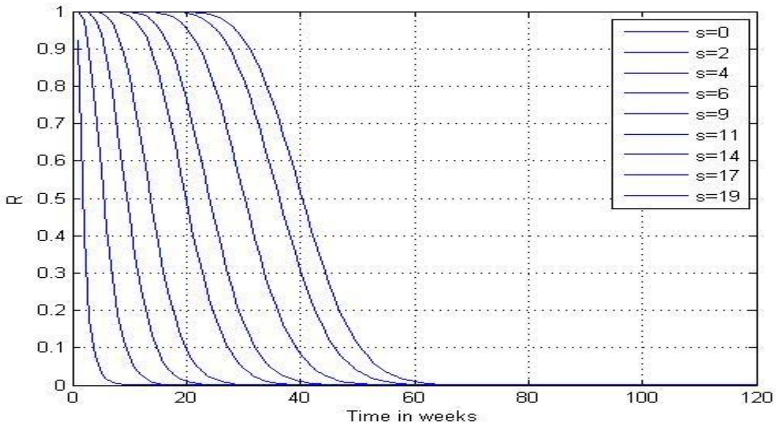

Figure 3 Reliability Values vs time for 128 X 128 Memory Module

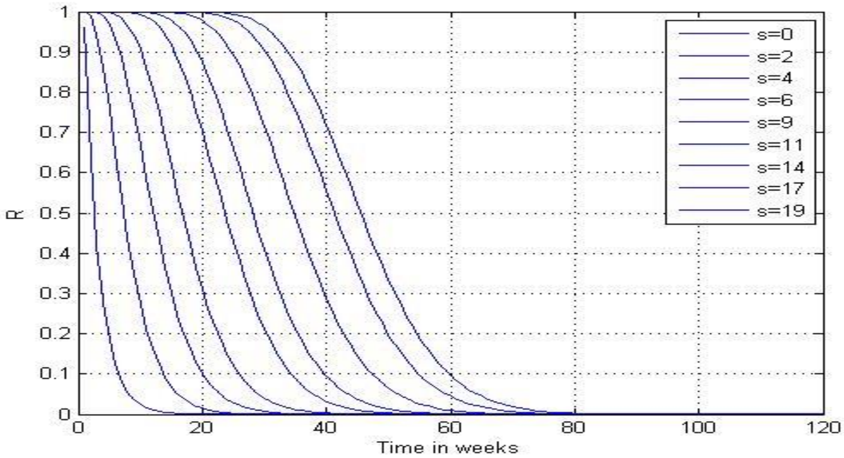

Figure 4 Reliability Values vs time for 256 X 256 Memory Module

Table 2 Reliability Values at the time given in weeks

Sl No	Memory Description	No.of spare columns	Reliability Values at the time given in weeks					
			1	10	20	30	40	50
1	128 X 128	0	0.959775	0.023847	0.000393	6.48E-06	1.07E-07	1.76E-09
2		2	0.999989	0.274572	0.01484	0.000505	1.40E-05	3.43E-07
3		4	1	0.668986	0.101761	0.00693	0.000318	1.16E-05
4		6	1	0.90694	0.310495	0.04043	0.003031	0.000163
5		9	1	0.993495	0.70237	0.212259	0.031952	0.00302
6		11	1	0.999269	0.87509	0.410933	0.094736	0.012862
7		14	1	0.999983	0.977812	0.716319	0.287842	0.065182
8		17	1	1	0.997488	0.904925	0.554833	0.198553
9		19	1	1	0.999528	0.962124	0.718468	0.334984
1	256 X 256	0	0.921168	0.000569	1.54E-07	4.19E-11	1.14E-14	3.09E-18
2		2	0.999977	0.07539	0.00022	2.55E-07	1.95E-10	1.18E-13
3		4	1	0.447542	0.010355	4.80E-05	1.01E-07	1.34E-10
4		6	1	0.82254	0.096407	0.001635	9.19E-06	2.65E-08
5		9	1	0.987032	0.493324	0.045054	0.001021	9.12E-06
6		11	1	0.998539	0.765783	0.168866	0.008975	0.000165
7		14	1	0.999967	0.956117	0.513113	0.082853	0.004249
8		17	1	1	0.994983	0.81889	0.307839	0.039423
9		19	1	1	0.999056	0.925682	0.516197	0.112214

6. CONCLUSIONS

As per the recent trends, the comparative silicon area occupied by memories in embedded systems has become nearly 95%. In addition, it is well known that faults show spatial locality in VLSI circuits. So reliability measurement for the fault-tolerant embedded memory system under fault clustering has been proposed and calculations carried out throughout the parametric simulation in this paper. Two sample memory blocks 128 X 128 and 256 X 256 have been taken and reliability calculations have been done for different values spare columns. The calculations equally apply for spare rows also.

REFERENCES

[1] Han, H., Touba, N. A., & Yang, J. S. (2017). Exploiting Unused Spare Columns and Replaced Columns to Enhance Memory ECC. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*

[2] Lee, H., Cho, K., Kim, D., & Kang, S. (2017). Fault Group Pattern Matching with Efficient Early Termination for High-Speed Redundancy Analysis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.

[3] Reddy, B. N. K., Vasantha, M. H., & Kumar, Y. N. (2016, July). A Gracefully Degrading and Energy-Efficient Fault Tolerant NoC Using Spare Core. In *VLSI (ISVLSI), 2016 IEEE Computer Society Annual Symposium on* (pp. 146-151). IEEE.

[4] Shyue-Kung Lu, Yu-Chen Tsai, Chih-Hsien Hsu, Kuo-Hua Wang, and Cheng-Wen Wu *"*Efficient Built-In Redundancy Analysis for Embedded Memories With 2-D Redundancy*"* *IEEE Transactions On Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 1, january 2006.

[5] M. Choi and N. Park, F.J. Meyer, E Lombardi V. Piuri "Reliability Measurement of Fault-Tolerant Onboard Memory System under Fault Clustering *" IEEE Instrumentation and Measurement Technology Conference Anchorage*, AK, USA, 21-23 May 2002.

[6] C. P. Low and H. W. Leong, "A New Class of Efficient Algorithms for Reconfiguration of Memory Arrays," *IEEE Transactions on Computers*, vol 45, No 5, pp. 614-618, 1996.

[7] N. Park and F. Lombardi, 'Repair of memory arrays by cutting," Memory Technology, Design and Testing, Proceedings International Workshop on, pp. 124—130, August 1998.

[8] K. Amdt, C. Narayan et al, 'Reliability of laser activated metal fuses in DRAMs," *Electronics Manufacturing Technology Symposium twenty Fourth IEEFJCPMT*, pp. 389-394, October 1999.

[9] D. M. Blough, "Performance Evaluation of a Reconfiguration Alogorithm for Memory Arrays containing Clustered Faults," *IEEE Transactions on Reliability*, vol 45, no 2, pp. 274—284,June 1996.

[10] D. M. Blough and A. Pelc, "A Clustered Failure Model for die Memory Array Reconfiguration Problem," *IEEE Transactions on Computers*, vol 42 ,NO 5, pp 518-528,may 1993.

[11] Y.Jeon,Y.Jun and S.Kim, " Column Redundancy Scheme For Multiple I?O DRAM using Mapping Table," *Electronics Letter*, Vol 36,No 11 , May 2000.

[12] R. J. McPartland, D. J. Loeper, et al, "SRAM Embedded Memory with low cost, FLASH EEPROM Switch Controlled Redundancy,"*Custom Integrated Circuits Conference,CICC,Proceedings of the IEEE*, Vol 36, No 11,pp.287-289, May 2000.

[13] T.Fichna, M.Gartner, F.Gliem, and F.Rombeck, "Fault Tolerance Of Spaceborne Semiconductor Mass Memories," Fault Tolerant Computing, Digest of papers, Twenty-eight Annual International Symposium on,pp. 408-413,1998.

[14] K.A Clark and B.W. Johnson, "A Fault Tolerant Solid State Memory for Space borne Applications, "proceedings of the Government Micro- Electronics Applications Conference pp. 441- 444, November 1992.

[15] T.P. Haraszti, R.P Mento,N.e.Moyer and W.M>Grant, "Novel Circuits for Radiation Hardened Memories,"IEEE Transactions on Nuclear science, vol 39,no 5,pp 1341-1351,October 1992.

[16] F.J.Meyer and D.k. Pradhan "Modelling Defect Spatial Distribution,"IEEE transactions on computers,Vol 38,pp 538-546,April 1989.

[17] S.Y Kuo and W.K.Fuchs, "Efficient Spare Allocation in Reconfigurable Arrays" IEEE design and test, pp 24-31,FEB 1987.

[18] C.H.Stapper,"On Yield, Fault Distributions, and Clustering of particles," IBM J.Res.Develop., Vol 30,NO 3,pp.326-338,May 1986.

[19] Mohammed Sirajuddin, Dr. D. Rajya Lakshmi and Dr. Syed Abdul Sattar. Clustered Conduction Of VOIP Routing Topology For 802.11 WLAN. International Journal of Computer Applications (IJCA), 1(1), 2013, pp. 15–21

[20] Manikandapirapu P.K.,Srinivasa G.R., Sudhakar K.G, Madhu D. Numerical Simulation Of Flow Modeling In Ducted Axial Fan Using Gaussian Quadrature Method. International Journal of Mechanical Engineering and Technology, 3(2), 2012, pp. 300–309.