DESIGN OF FLASH ANALOG-TO-DIGITAL CONVERTER USING HIGH GAIN COMPARATOR

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ABSTRACT
This paper describes the designing of Flash ADC using High Gain Comparator. ADC is an important building block in the modern era of communication. It is widely used in radar systems for subsequent signal processing. An analog to digital converter is used to convert a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude. In this project a 4-bit Flash ADC has been designed using 180nm technology. The basic building blocks of ADC are resistor ladder, comparator, and encoder. Firstly a resistive ladder circuit has been designed. Then we have designed analog comparator which is used to compare input signal with reference signal. Input signal is given in analog form and reference signal is generated by ladder. The output of comparator is given to the encoder. Encoder will convert the input (thermometer code) to binary output. In order to meet the requirement of low power and high speed, 180 nm CMOS technology has been chosen for design and simulation. The power dissipation of the designed circuit is 5.04 mW. The simulation has been performed with Cadence virtuoso using GPDK 180nm technology.

Keywords: Analog-to-Digital Converter (ADC), CMOS Technology, Comparators, LSB, High Gain.


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1. INTRODUCTION
In today’s world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high resolution and high-speed
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applications. In order to achieve digital signal, we need to convert the analog signal into digital form by using a circuit called analog-to-digital converter. Whenever we need the analog signal back, digital-to-analog converter is required. Analog to digital converters are vital to many modern systems that require the integration of analog signals with digital systems. The applications of digital system can range from audio to communications applications to medical applications. These converters are implemented using a variety of architectures, sizes and speeds. The demand for the converter is oriented on area, speed, power of the converters. This has led to the investigation of alternative ADC design techniques. Analog-to-digital converters (ADCs) are used to convert real world analog signals into digital representations of those signals. As we know that the digital signal processing can then efficiently extract information from the signals. ADCs find use in communications, audio, sensors, video and many other applications. High-speed (multi-GHz sampling rate), low-resolution (4- to 8-bit) ADCs are used in oscilloscopes, digital high-speed wired and wireless communications and radar. Flash and time-interleaved ADCs architectures are typically used for high-speed applications. There are various types ADC architectures in which first is pipeline ADC. Its operating speed is high but below flash with medium resolution. Second ADC architecture is SAR ADC. It is suitable for low power and medium-to-high resolution applications with moderate speed. Third ADC architecture is Sigma-delta ADC. It is suitable for high resolution and low speed applications. Fourth ADC architecture is Flash ADC. It can operate at high speed and low resolution. So we can say that Flash ADC is the fastest ADC in comparison with other ADC architectures. The flash ADC is the best choice in high speed low resolution applications. It is highly used in high data rate links, high speed instrumentation, radar, digital oscilloscopes and optical communications. Since flash ADC is operating in parallel conversion method, maximum operating frequency in the range of gigahertz is possible. Comparator design is also a challenge for design of 4-bit Flash ADCs. Here we have used the analog Comparator in the comparator block.

2. ANALOG TO DIGITAL CONVERTER

Analog to Digital Converter (ADC) is a device that accepts an analog value (voltage/current) and converts it into digital form that can be processed by a microprocessor. Figure 2.1 shows a simple ADC with analog input and digital output bits. Analog to digital converters are the basic building blocks that provide an interface between an analog world which accepts an analog value (voltage/current) and converts it into digital form that can be processed by a microprocessor. As it is the main block in mixed signal Applications, it becomes a bottleneck in data processing applications and limits the performance of the overall system. Different architecture of ADCs includes Flash, Sigma-Delta, Pipeline, Successive Approximation and Dual Slope ADCs.

Figure 1 Block Diagram of ADC
3. DESIGN OF THE PROPOSED FLASH ADC

Flash ADC’s have parallel architecture and is the fastest ADC among all the other types and are suitable for high bandwidth applications. A typical flash ADC block diagram is shown in Figure 2 and it can be seen that 2N – 1 comparators are required for an “N” bit converter. The resistor ladder network is formed by 2N resistors, which generates reference voltages for the comparators. The reference voltage for each comparator is one least significant bit (LSB) less than the reference voltage for the comparator immediately above it. When the input voltage is higher than the reference voltage of comparator it will generate a “1”, otherwise, the comparator output is “0”. The output of all the 2N-1 comparators is in the form of thermometer code. It is known as thermometer code because it is very much analogous to mercury thermometer. In the mercury thermometer, mercury rises only up to or below a specified level of temperature. No mercury is present above the specified temperature. Similar is the case with the output of the comparators.

![Figure 2 Block Diagram of Flash ADC.](image)

Various types of ADC are compared as follows;

**Table 1** Comparison of Various ADCs

<table>
<thead>
<tr>
<th></th>
<th>FLASH</th>
<th>SAR</th>
<th>PIPELINE</th>
<th>SIGMA DELTA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Key Features</td>
<td>Ultra high speed when power consumption is not the primary concern</td>
<td>Medium to high resolution (8 to 15 bit), up to 3 Mbps, low power, smaller size</td>
<td>High speed up to 100 Mbps, resolution (8 to 16 bit), lower power consumption than Flash ADC</td>
<td>High resolution, low to medium speed</td>
</tr>
<tr>
<td>Conversion method</td>
<td>Requires 2N-1 comparator for N bit conversion</td>
<td>Binary search algorithm, internal circuitry runs higher speed</td>
<td>Small parallel structure, each stage works on one to few bits</td>
<td>Oversampling ADC, 5-60 Hz rejection, programmable data output</td>
</tr>
<tr>
<td>Encoding Method</td>
<td>Thermometer encoding</td>
<td>Successive approximation</td>
<td>Digital correction logic</td>
<td>Oversampling modulator, digital decimation filter</td>
</tr>
<tr>
<td>Conversion time</td>
<td>Conversion time is constant</td>
<td>Increases linearly with</td>
<td>Increases linearly with</td>
<td>Trade off between data</td>
</tr>
</tbody>
</table>

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Some of the basic terminologies used in ADC design are explained below,

**Input Signal Bandwidth:** The range of frequency over which input signal can pass without distortion in amplitude, is known as signal bandwidth. If a sine wave is used as input signal, then bandwidth is defined as the range of frequency over which amplitude reduces to 70.7% of its original amplitude.

**Resolution:** Resolution is defined as the smallest change in the magnitude of input signal which will be observed at the output.

\[
\text{Resolution} = \frac{V_{\text{FSR}}}{2^N - 1}
\]

**Sample Rate:** Sampling is the first step in the process of analog to digital conversion. Sample rate is defined as the number of samples taken per seconds. Nyquist theorem gives the relationship between the sampling frequency and maximum signal frequency. According to this signal frequency must be at least equal to or greater than twice of the maximum signal frequency. This theorem is used to reconstruct the signal properly.

**Quantization Error:** Quantization is defined as the process of making the signal discrete in both time and amplitude domain. When an analog signal is converted to digital signal, a certain amount of uncertainty exist. This uncertainty is known as quantization error.

**Signal to Noise Ratio (SNR):** Signal to noise ratio is the measure of the noise performance of a circuit. Higher is the SNR, better is the noise rejection capability of the circuit. It is defined as the ratio of signal power to the noise power. It can be represented as:

\[
\text{SNR} = 10 \log_{10}(P_{\text{signal}} / P_{\text{noise}})
\]

Where \(P_{\text{signal}}\) is the signal power and \(P_{\text{noise}}\) is the noise power.

**Effective Number of Bits (ENOB):** ENOB is another important parameter which is used to measure the actual performance of an ADC. It defines the conversion bit of an ADC. ENOB is related with SNR with the relation shown below

\[
\text{ENOB} = \frac{(\text{SNR} - 1.76)}{6.02}
\]

**Spur- Free Dynamic Range (SFDR):**

SFDR is defined as the ratio of the power of fundamental frequency signal to the power of the largest spur signal present in the output of ADC. SFDR represents the fidelity of an ADC. SFDR arises due to non-linearity. SFDR can be calculated using the formula:

\[
\text{SFDR} = \text{Signal (db)} - \text{largest spur (db)}
\]

**Differential non-linearity (DNL):** DNL is a measure of separation between adjacent levels measured at vertical jump. DNL measures any deviation from one LSB. As follows

![Figure 3 Differential Non- Linearity Measurement](image-url)
4. PROPOSED FLASH ARCHITECTURE
In flash ADC an array of comparators compares the input voltage with a set of increasing reference voltages. All flash ADCs comprises of following three blocks;

**Resistor Ladder:** Resistor ladder is used to generate the reference voltages for the comparators. It is assumed that the feed through at nodes ref-low and ref-high is negligible due to proper decoupling. Maximum feed through will occur on the mid node.

**Comparator:** A comparator is used to detect whether a signal is greater or smaller than reference signal. Various comparator include multiple stage comparators, Regenerative Comparators (positive feedback), Resistive Driving Comparators and fully differential Dynamic comparators.

**Encoder:** Encoder will convert the input (thermometer code) to binary output.

![Figure 4: ADC Architecture](image)

5. SIMULATION AND EXPERIMENT RESULT

![Figure 5: Two-Stage Open-Loop Comparator](image)

For M1- saturation region- W/L=4.266
M2 is same as M1 because of current mirror
M3- saturation region – W/L=13.02
M4 is same as M3 because of current mirror
M5 –W/L=13.13
M6-W/L=172.82
M7-W/L=82.64
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Figure 6 Schematic of FLASH ADC

Figure 7 Output of Flash ADC for Vpwl input at 1MHz

Figure 8 Output of Flash ADC for Vpwl input at 10 Khz
From the above the following are the observations

### Table 2

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Comparator Type</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Two Stage Open-loop Comparators</td>
<td>5.04 mW</td>
</tr>
<tr>
<td>2</td>
<td>Resistive Driving Comparators</td>
<td>7.031 mW</td>
</tr>
<tr>
<td>3</td>
<td>Fully Differential Dynamic Comparator</td>
<td>8.515 mW</td>
</tr>
</tbody>
</table>

### 6. CONCLUSIONS

FLASH ADC has been designed using 180nm technology and with maximum power supply of 1.8 V. As power dissipation of any circuit plays a major role in the designing procedure so power dissipation must be as small as possible. The power dissipation of the designed ADC is 5.04 mW. As Op-Amp is used as comparator, it provides sufficiently large gain and gain bandwidth product. So this design can be used to operate at higher range of frequencies. The encoder is designed using multiplexors, so provides faster switching as compared to other comparators. The area required by the ADC can be calculated by making its layout. As resistors require larger area as compared to MOSFET, resistor ladder can be designed using nMOS as resistors or pMOS as resistors. But it will require large degree of precision while setting the various reference voltages. Flash ADC can be designed using CMOS inverter as comparator. This will require less area and less power consumption as there is no need to design resistive ladder network. But defining threshold voltage of each comparator is the biggest problem. So designed ADC is superior to other Flash ADC architectures in terms of functionality i.e speed and inferior in terms of power consumption and area.

### REFERENCES


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