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VLSI BASED IMAGE COMPRESSION ARCHITECTURE USING DWT

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ABSTRACT

In image processing one of significant perspective is the image compression. It is concerned in reducing the quantity of fundamental element to represent of an image. An immense memory and high data transfer capacity are required for transmission of pictures continuously. Hereafter to build the organization capacities of winning organizations in a successful way and furthermore to make the interest for capacity to an economical level, image compression gives a quick solution for this arrangement. In this proposed work, an effective discrete wavelet transform (DWT) is designed for compression of image by utilizing fundamental cell strategy and a streamlined controller pathway laterally with a capable design architecture is suggested. The architecture design is thought by reasonably interconnecting the units and is realized in Verilog HDL. The task complier is been utilized to synthesize and confirm the design functional practically by utilizing the EDA tool. The result of the approach shows decline in power use, repetition in memory utilization, high-throughput and less latency contrasted with other existing techniques.

Key words: Convolution, DWT, Image compression, Verilog HDL, VLSI design.

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1. INTRODUCTION

An important role is been played by compression techniques based on 3 level Decomposition Discrete-Wavelet-Transform (3D-DWT) in applications like multi-media, medical imaging and broadcasting media. The chief purpose of compressing is to eliminate unnecessary data to a substantial level such a way the data be able to save up, handled, and channelized [1]. The 3D DWT can be used to achieve both temporal and spatial dominion solidities using audiovisual

encoder. The main advantages of incorporation wavelet aimed at audiovisual encoding are removal of artefacts blocking, scalability and with better quality. With the increase in dimension of audio-visual formats gradually, software founded compression methods practice great complication in calculation and necessitate mammoth memory. To obtain the compressed images with better PSNR and compression ratios, the wavelet transform is the best method in image compression applications [13]. Precise hardware construction aimed at 3D-DWT is essential to procedure huge magnitude audiovisual structures for augmented area, power in addition regularity [5]. Similarly, the consumption of memory should be less.

Earlier, a range of 2D in addition 3D-DWT proposals are industrialized. Convolution and lifting are the basic principles of most of these designs of DWT proposed [2]. The general drawback of all these major DWT designs is less sampling rate, great memory necessity besides composite circuitry. Memory and arithmetic define the complication of DWT carrying out. The multipliers and adders define the arithmetic portion of DWT, meanwhile the length of input image defines the complexity [6]. Temporal, transpose and intermediate memory parts altogether forms the memory unit.

In addition, the input frame resolution of input imagery decides the memory size required. The size of frames is increasing in such a way that the size is not compatible with the DWT word length [4]. This is major reason; the memory plays a vital role for instrumentation of DWT [4]. The convolution founded DWT methodologies provide a good computation time, though they require a huge number of multipliers and adders which increases the design area even [7]. Meanwhile these parameters are well taken care in the lifting founded DWT designs and also better restoration, on place calculation and good processing in time domain [8]. The lengthy critical path makes the major drawback of this lifting method of DWT structure. Flipping approach implemented for the elating DWT constructions affords decrease in crucial track with the charge of augmented memory [9]. A moment ago, great amount of flipping and lifting 3D-DWT constructions are projected to diminish precarious path suspension. Maximum of 3D-DWT assemblies institute 2D-DWT components that are engaging 1D-DWT in vertical manner and smear them in horizontal manner [8]. In numerous lifting founded 3D-DWT constructions, lessening of crucial track is taken attention on 1D-DWT glassy. Additionally, they remain active further to construct 3D-DWT designs.

A large portion of the 3D DWT constructions, establish 2D DWT units which are utilizing 1D DWT in the row wise manner and put on them in the column wise manner. In many cases lifting scheme-based 3D DWT constructions reduces the critical path by considering essence of 1D DWT and further, by utilizing these coefficients to develop 3D DWT design. This procedure accomplishes decrease in memory [7]. Pre-calculated flipping constant founded 3D-DWT construction is employed in few methodologies [11]. Few of the equivalent and memorial effective lifting 3D-DWT constructions are realized [12 and 13]. Sampler ratio is augmented by administering 1D-DWT components in parallel handling. Maximum of constructions revealed overhead are employing transfer remembrance for scheming one smooth of 2D-DWT component and great size progressive memorial to project one glassy of 3D-DWT construction [10].

A VLSI architecture for 3D DWT is proposed, for efficient utilization of the hardware which results in a better efficiency. The architecture processes on image to achieve better hardware utilization. In this proposed work the raw image is correctly scanned into the strategy unit in a correct format. The efficient embedded technique is rendering to optimize the structure of 1D DWT, and this receives a raw image as an input and designed to produce the lower and higher frequency constituents of original data as an output which are obtainable alternately. Establishment on this 1D DWT structure, a 2D DWT architecture has been further proposed by incorporating high pass and low pass units with the composed of horizontal and vertical filter

modules. Both are employed in parallel manner by achieving the 100% utilization of hardware structure. The proposed 2D DWT construction is termed as a fast processing component (FPC), which is being used to create the L-L, L-H, H-L and H-H band DWT coefficients. The L-L band DWT coefficients contain the significant information, which is being considered as transformed feature coefficients, and in turn reduces the dimension of the image [15]. The combination of FPC with the 1D DWT basic cell architecture to form 3D DWT architecture that can accomplish three level decomposition of image happening around in interior time clock sequences. The design of architecture can be extended on behalf of other DWTs. Furthermore, the modest and effectual 3D DWT construction is suggested by adopting the parallel working among eight sub bands, which accomplish three level decomposition of image happening around in interior time clock sequences; therefore, it is termed as high-speed architecture. The outturn rate is better when compared with the other 3D architecture, with no additional hardware, consequently it has better execution concerning hardware cost versus throughput rate. When contrasted and the works detailed in past writing, the proposed structures for 3D DWT are effective among outturn rate, control multifaceted nature, hardware cost, output latency.

The proposed paper is orchestrated in the following manner. DWT is explored in the section 2. Detail discussion of the proposed research works includes test images database, feature extraction and the basic cell, flipping cell, 1D DWT module, 2D DWT module which are essential to structure the 3D DWT suggested in section the 3. Implemented system outcomes and its performance measures are compared with CR, PSNR, SSIM, MSE are conveyed in the section 4. Proposed work Conclusion are made in the section 5.

2. DISCRTE WAVELET TRANSFORM (DWT)

Images contains of pixels which remain organized in dual dimensional mediums, every pixel characterizes the alphanumeric correspondent of image concentration. In longitudinal dominion neighboring pixel standards are extremely associated and henceforth terminated. In instruction to compressing imageries, such terminations prevailing amongst pixels requires to be eradicated. DWT mainframe transmutes the altitudinal province pixels into frequency province material that are characterized in numerous sub groups, signifying dissimilar time gage and frequency facts.

The sub group encoding of wavelet-transmute is castoff to produce a reckless calculation, that assistances to diminish the calculation time and possessions. Imageries can be characterized at dissimilar measures with native contrast variations with superior scale assemblies by means of wavelets [5]. The indicator in DWT is signified by means of vigorous sub group breakdown, deprived of any restriction. Its proposals healthier energy computation than DCT deprived of any obstructive article. DWT division constituent into abundant frequency groups named sub-bands identified as

Mutually vertical and horizontal low-pass – LL

Low-pass with horizontal and high-pass with vertical - LH

High-pass with horizontal and low-pass with vertical - HL

Mutually vertical and horizontal high-pass –HH

With the help of HPF and LPF, the input imageries are decayed into high and low-pass constituent's bountiful increase to principal glassy of grading. This procedure is sustained till several grading are attained.

From past several decades, many hardware designs are obtained for implementation of 1D/2D/3D DWT and IDWT for many kinds of applications. Two categories of designs were developed, viz. (i) convolution based (ii) lifting-based. Lower throughput, greater memory

constraint and complex regulator circuits are the major difficulties existing with the much of the designed architectures.[18] [19].

In general, two major components called arithmetic and memory component are used to define the complexity of the circuit. Adders and multiplier are present inside the arithmetic component, in case of memory component temporal memory and transpose memory. Depending upon the DWT filter length, the complexity of the arithmetic components decided. The image dimensions decide the memory components size. The overall complexity of DWT architecture increases with the increasing resolution, dimensions of image is actually high compared to the length of the DWT filter coefficients [20].

The advantages of using DWT:

- Implementation makes easier.
- Image is analysed for different frequency with varied resolutions.
- For analysis and synthesis enough, information is available.
- Complexity is reduced.
- Decomposition structure with approximation and detail coefficients.

3. PROPOSED RESEARCH

This section illustrates the innovative image compression based on VLSI architecture DWT construction, which is intended by appropriately interlocking the ultimate basic cells and flipping cells for three level decomposition using DWT. The proposed system is examined by database test images to equate concluding features.

3.1. Test images Databases

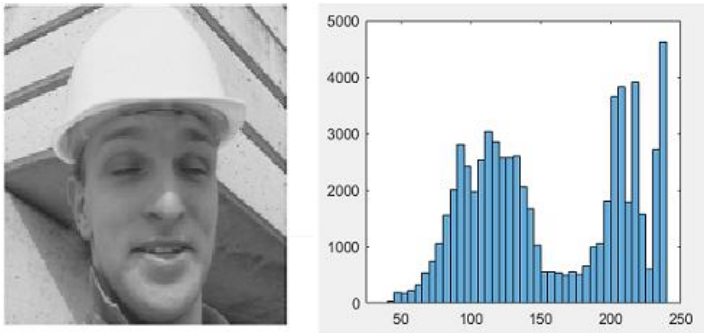
The publically available test images are utilized to test the suggested system model. The system model is experimentally verified by taking the different kinds of images, which are publically available datasets. So, to reduce the required hardware complexity, the normal gray scale images only eight-bit pixel lengths are considered. The all test images of databases are of standard size 256x256 in the proposed method, which is shown in Fig 1.

Figure 1 Test images database

3.2. Feature Extraction

The Histogram of an image is an important feature extraction in the application of image compression algorithm. Histogram is utilized for spatial domain features, by drawing the recurrence of event of pixels for different intensity of an image. It shows the absolute pixels number relating to intensity level of each pixel of an image. The axis x represents all accessible gray levels pixel intensity in the image and the axis y represents the quantity of pixels

comparing to every intensity level in the image. The white pixel intensity is 255 value and the black pixel intensity value is zero. The sample image and its relating histogram are as appeared in Fig 2. The given input image histogram contains practically almost all pixel levels intensities.



(a) Image (b) Histogram

Figure 2 Histogram of an image

3.3. Proposed Construction

Proposed design for three level decomposition utilizing DWT is obtain by combination of the constituent components, for example, basic cell components and flipping cell components. Development of every one of these individual parts and the strategy to get one level, two level and three level decomposition of the 3D DWT is discussed. The complete view about three level decomposition working of the distinctive functional blocks is as per the following.

The 1D DWT is the basic functional unit of 2D-DWT and 3D-DWT. 2D-DWT does row operation and column operation as well. 1D-DWT does only column operation. These L, H are again spitted in to HH, Hl, LH and LL through 2D DWT process, the outputs of 2D-DWT is further processed and decomposes to eight cells, with one low frequency and seven great frequency groups. HH, HL, LH and LL samples are decomposed to HHH, HHL, HLH, LHH, LDL, LLH and LLL which is revealed in Fig 3, which shows the pin layout of the proposed architecture. The DWT design is also been proposed by many VLSI methodologies.

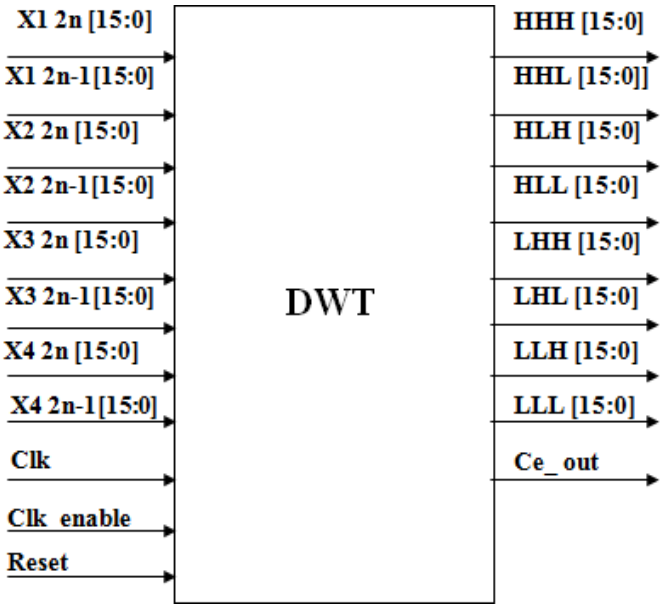


Figure 3 Pin Layout of Proposed Architecture

Let us consider ‘A’ as input imagery that have prefixed pixel values.

Consider, A = [A (1), A (2) ... A (2n)] remain a selection of dimension 2n. The poly stage decay is used in the method, which splits A into 2 sub-groups, with a dimension *N*. The input image pixels are splatted into even and odd number of pixels during divided phase of technique.

$$A_o = [A (1), A (3), A (5) ... A (2n-1)]$$

$$A_e = [A (2), A (4), A (6) ... A (2n)]$$

Proposed DWT construction consist of dual link barriers, each one for even and the other for odd data extraction. 3D DWT does the row and column operation, and row operation, splits the sample pixels in to eight frequency co-efficient as appeared in the figure 3. Proposed architecture is consisting of a group of 1D DWT components. The pin layout of the 1D DWT is as shown in Fig 4. Here, explains the design of 1D DWT by means of basic-cell. Two adders, one multiplier and two registers are combined together to form the basic cell, this assembly of basic cell is revealed in Fig 5. a1, a2, and a3 are the 3 input samples are given to the BFC and flipping constant (K_f) is multiplied to a1 and further summed with remaining two sections (a2 + a3). Two outputs b1 and b2 are obtained by pipelining registers R1 and R2. Four BCs are connected in cascade and A, B, C, and D remain as flipping constants, are been multiplied for output got from cascade connected BC's respectively. K_0 and K_1 remain as regularizing coefficients. Flipping constants and conforming standards remain specified in Table 1. Additionally, the fourth BC outcome is multiplied with flipping cell, which will produce the 1D-DWT flipping outcome after scaling and normalizing. The Fig 6 displays the representation of flipping cell and the structural configuration of 1D DWT component is shown in figure 7. For the specified arrangement of input sources, each 1D DWT produces a couple of sub- bands in particular low-pass (L) and high-pass (H).

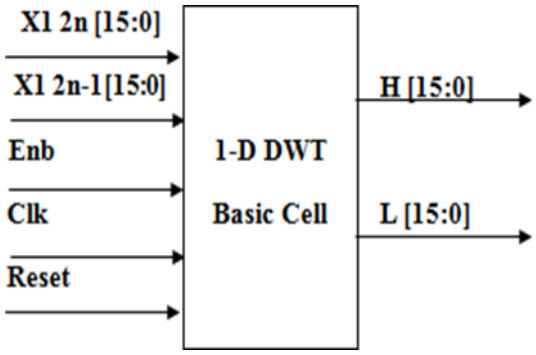


Figure 4 Pin Layout of 1D DWT

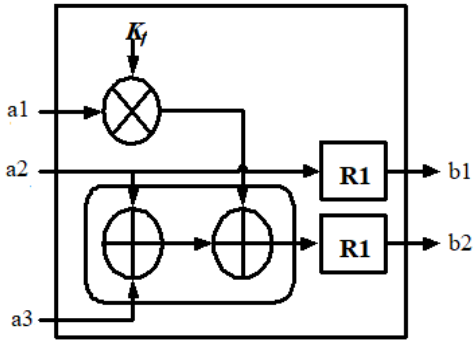


Figure 5 Structure of Basic Cell

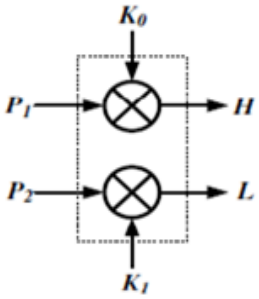


Figure 6 Structure of Flipping Cell

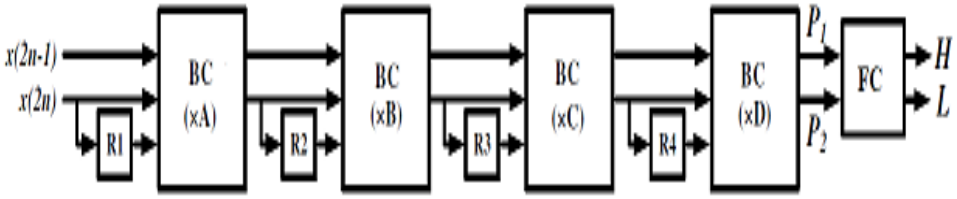


Figure 7 Structure of 1D DWT

Table 1 Flipping Coefficients with Their Standard

Flipping Constants	Standard
A	-631453
B	0.742740
C	-667057
D	0.637433
K_0	2.580687
K_1	1.939971

The structure of the 2D DWT module is shown in Fig 8. Each 1D DWT produces two sub groups, namely low and high pass with the given inputs. A couple of low and high pass units is arranged in an array in the upcoming block. A pair of sub bands (HH & HL) are obtained by the High-pass division after processing comprehensive transitional constituents. Similarly, low-pass division generates sub-bands (LL & LH) based on estimated intermediate modules. The sub band yields from this unit are scaled to construct 2D DWT section. Each 2D DWT section creates four sub groups (LL, LH, HL, and HH). The coefficient constants K, α, β, γ and δ remain as lifting coefficient and their values as shown in Table 2. Both 1D and 2D DWT work simultaneously.

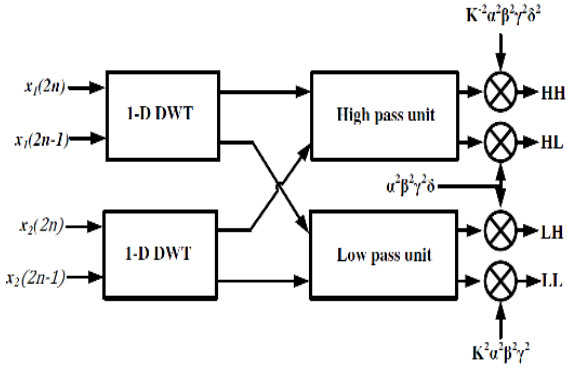


Figure 8 Structure of 2D DWT

Table 2 Lifting Constants and Their Standards

Lifting Constants	Standard
α	-1.58513535
β	-0.05288011
γ	0.883911175
δ	1.148604498
K	0.443406862

Suggested 3D DWT VLSI architecture which is shown in Fig 9, contains an array of 2D DWT modules. Four sub bands are generated from each 2D DWT module. These eight sub bands (LL_0 to HH_1) inputs to the next module which consists of four 1D DWT in an array fashion and this in turn produces 3D DWT output sub bands. The subsequent module is an array of 1D DWT modules. Each one of the 1D DWT unit yields an approximation and detail sub groups. Sequential memory buffer isn't needed unlike in different other architectures, because of these cross associations in the development of the 3D DWT structure. Entirely approximation and detail sub band segments are considered and the collectively total output develops eight sub groups from LLL to HHH bands of the 3D DWT of the architecture.

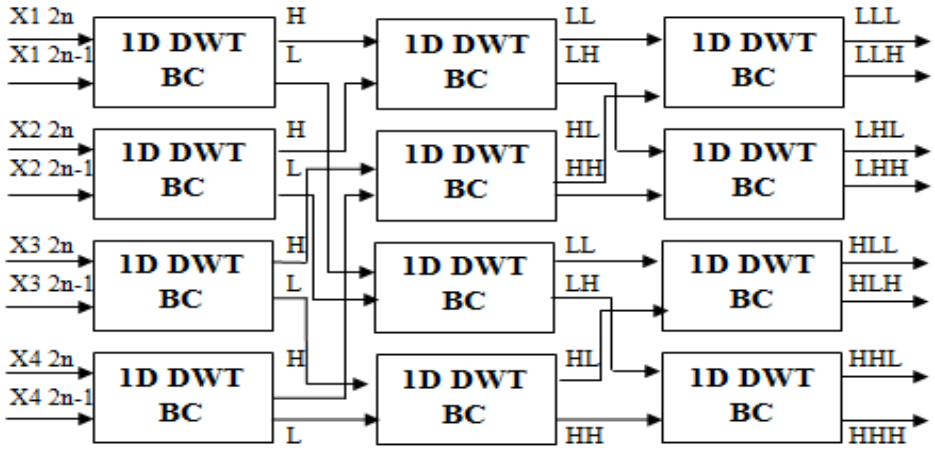


Figure 9 Proposed 3D-DWT VLSI Architecture

The details algorithm of the proposed system has been explained in the Table 3. The input image of size 256*256 decomposed into one, two and three levels are shown in Fig 10.

Table 3 Proposed Algorithm

Input: The test images of databases are of standard size 256x256

Output: Compressed 128x128 output & Reconstructed 256x256 image and evaluation of performance parameters.

1.The test images of size 256x256 is used are used, created binary values using Matlab.

2. The values are translated to Xilinx Platform; the DWT is applied on after pre-processing of an image and three-level LLL band of size 128x64 considered.

3.The LLL band & LHL band is combined to form a compressed 128x128 compressed image. The compression ratio of 0.75.

4. the inverse DWT is applied to get the reconstructed image 0f size 256x256.

5.The MSE, PSNR& SSIM is used to find the differences between a database and reconstructed images to exam the proposed model.

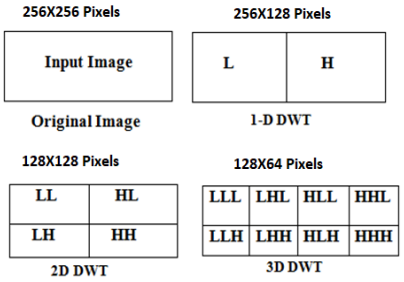


Figure 10 Image decomposition in 1D, 2D and 3D-DWT

3.4. Implementation results

Proposed 3D-DWT architecture design is comprehended as RTL level in Verilog-HDL and confirmed their functional correctness in Modelsim Simulator by writing the test bench. The DWT coefficients should be represented with an enough number of bits to avoid overflow because of increase in number of decompositions stages the dynamic range of DWT coefficient increases. To improve the SNR the additional bits to represent the fractional part of the DWT coefficients are incorporated in the proposed system. The proposed work uses 16 bits to represent the DWT coefficients and the corresponding results are also represented in 16 bits.

The architectures scheme is synthesised for Xilinx's Virtex IV FPGA XC4vfx20. The 3D implementation is achieved with the three stage DWT utilizes 4704 logic slices out of which available 8544 slices in the given FPGA and can applied the DWT on images with 8-bit grey scale-levels of sizes up to 256*256 at 88.798MHz using the available built-in multipliers and RAM blocks in the FPGA. The synthesized designs were then placed and routed. The Fig 11 shows RTL schematic view of structured 3D-DWT. DWT module consists of BFC's and each BFC consists of clock, reset, clock enable, odd and even inputs and each BFC produces the two outputs. Even in and odd in separated by the 256*256 pixels. Clock, Reset and Clock enable are the control inputs of the designs. $x_{12}n$ [15:0], $x_{22}n$ [15:0], $x_{32}n$ [15:0], $x_{42}n$ [15:0] are even pixels and $x_{12}n\_1$ [15:0], $x_{22}n\_1$ [15:0], $x_{32}n\_1$ [15:0], $x_{42}n\_1$ [15:0] are odd pixels. Outputs are HHH [15:0], HHL [15:0], HLH [15:0], HLL [15:0], LHH [15:0], LHL [15:0], LLH [15:0], LLL [15:0].

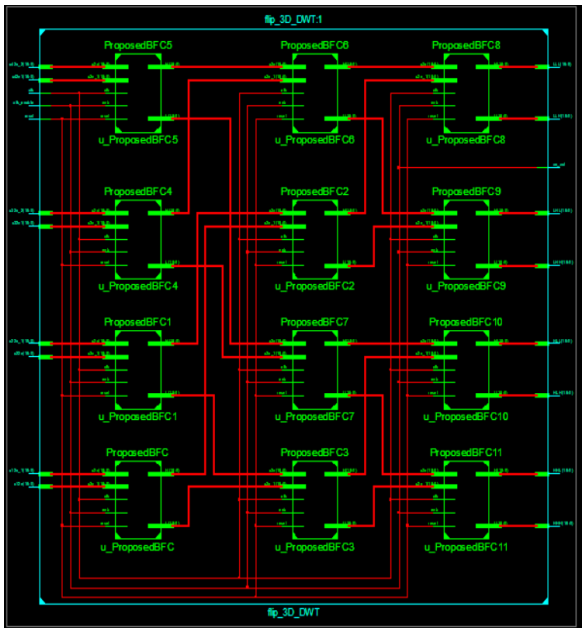


Figure 11 RTL Schematic view of 3D-DWT

The benefits in memory and calculation speed can be identified in the proposed methodology by not compromising throughput ratio. The Table 4 displays the comparison parameters such as count of slices cast off and count of flip flops used for 3D-DWT to compare performance. The timing report for the design as shown in the Table 5. As per the structure, the projected algorithm 3D-DWT design is modeled in Verilog HDL for 256*256 pixels standard foreman image, which is an input image shown in Fig 12.

Table 4 Synthesis Report

Target Device xc4vfx20-12ff672			
Resources	Number of Usage	Number of Accessible	Percentage of Utilization
slices	4704	8544	55
flip-flops slice	1554	17088	9
Four input LUTs	8916	17088	52
Bonded IOBs	260	320	81
GCLKs	1	32	3
DEP48s	32	32	100

Table 5 Clock Timing Report

Maximum time required for combinational path delay	6.047ns
Required speed Grade	-12
Maximum for output after the clock	11.357ns
Minimum time period requirement	11.262ns
Minimum time required for input appearance before clock	6.904ns
Maximum required frequency	88.798MHz

Figure 12 Foreman Image (256x256)

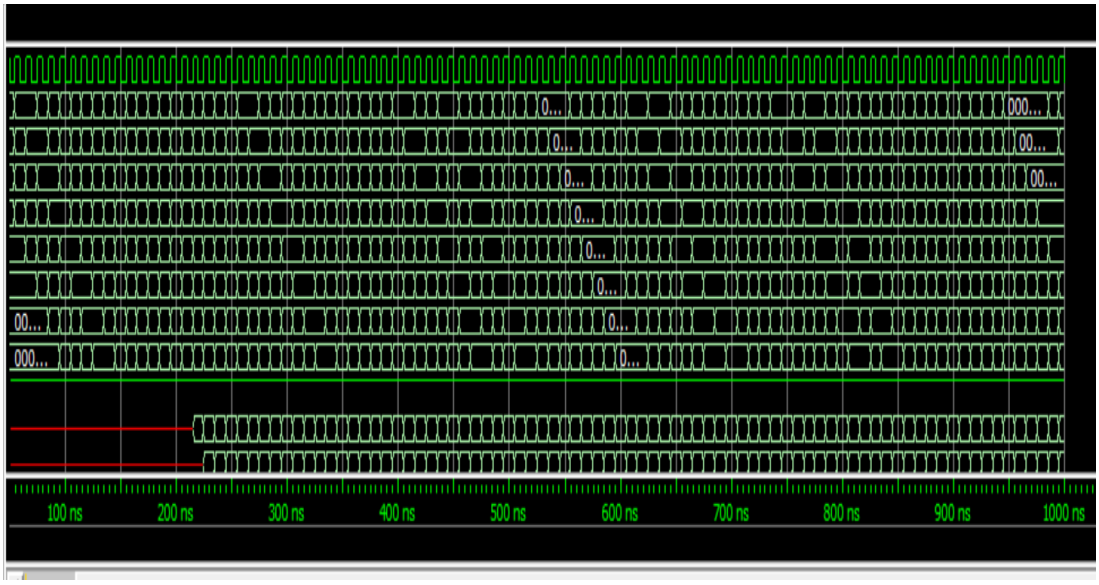


Figure 13 Simulation waveform

Fig 13 shows the simulation waveforms for the proposed VLSI architecture, which is done with Modelsim simulator. By using this method, the size of image should be reduced but their resolution and quality should be maintained at good without losing any data information. The three-level decomposition output is shown in Fig 14; its respective eight different bands are from LLL to HHH, which are associated to 3D DWT units are shown Fig 15.

Figure 14 DWT of output Image

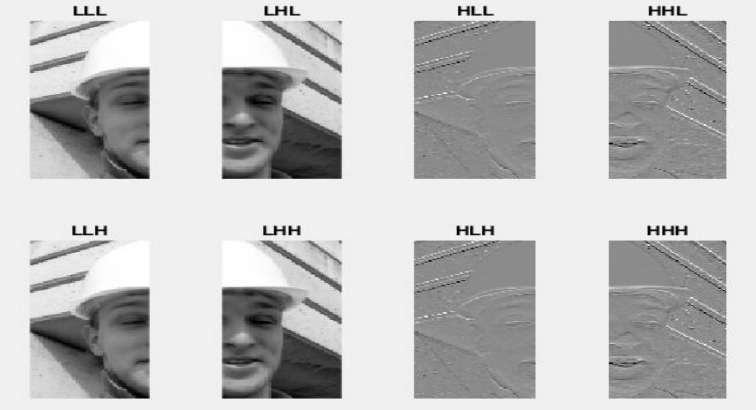


Figure 15 Eight Sub bands in the compressed output image

The original input image and the compressed image size 128x128 are as shown in Fig 16, a is formed by combining the LLL &LHL sub bands.

Figure 16 Compressed Output

The Percentage of achieved compression ratio is 0.7500.the CR is defined as follows.

Compression Ratio (CR): The ratio of original input size of the image with the compressed size of the image is known as the compression ratio (CR).

Apply the inverse discrete wavelet transform (IDWT), to get the reconstructed output image is shown in figure 17. This IDWT process is done by generating the Matlab code, which is helpful to get reconstructed output image and after getting the output image the pixel value should be same as the input image pixel value. The MSE and PSNR are calculated as the evaluation parameters. They are defined as follows.

Peak Signal to Noise Ratio (PSNR): The ratio between the noise and the peak signal is known as Peak Signal to Noise Ratio (PSNR).

Structural similarity index (SSIM): SSIM is the HVS based quality Metric. By multiplying the luminance, contrast and the structural term of an image we get the overall index called Structural Similarity (SSIM).

Figure 17 Reconstructed Image

The Error difference between the reconstructed image and the input image is shown in figure 18.

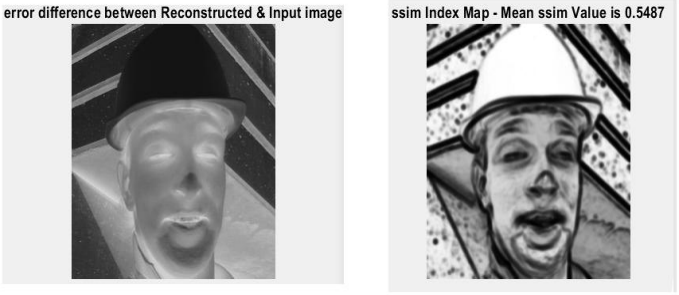


Figure 18 Error Difference & SSIM

The evaluation parameters such as compression ratio, PSNR and SSIM values for the 3D DWT of the tested gray-level images are recorded in Table 6.

The outcomes for unalike input images have been tested and generated respective outputs and compared its parameters of all tested images are tabulated in the Table.6.

Table 6 Numeric Results

Parameters	cameraman	Butterfly	Fence	foreman
CR	0.75	0.75	0.75	0.75
MSE	15.9613	15.9680	15.9444	15.9687
PSNR	+24.07 dB	+24.07 dB	+24.08 dB	+24.07dB
SSIM	40.7441	26.9204	26.5594	54.8703

4. CONCLUSION

The proposed work approach is to reduced power and area through using flipping 3D-DWT design. A collecting 1D-DWTcomponents are utilized to associate the structure to form a group of 2D-DWT, which doesn't utilize swap memory. The setup doesn't need the temporal-memory to structure the 3D-DWT design. This designed architecture has been utilized to confirm practically to verify functionally, in addition to synthesize and to implement the system. By the investigational aftermaths, 3D-DWT approach remains considerable a better design structure configuration once contrasted with present day related design. Similarly, proposed design is an improvement deprived of creation any negotiation by throughput ratio and more prominent to use for procedure greater visual frame designs.

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