NOVEL CIRCUIT REALIZATIONS OF NEURON ACTIVATION FUNCTION AND ITS DERIVATIVE WITH CONTINUOUSLY PROGRAMMABLE CHARACTERISTICS AND LOW POWER CONSUMPTION

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ABSTRACT

This paper presents novel circuit configurations to realize Neuron Activation Function (NAF) and the Derivative of Neuron Activation Function (DNAF) with low power dissipation. The circuits realize NAF and DNAF simultaneously with programmable characteristics. In the proposed configurations, tan sigmoid and log sigmoid NAFs and their derivative can be obtained from the same circuit simultaneously. Slope and threshold levels of NAF can be continuously varied and corresponding DNAF and its scaled versions can also be obtained. Monte carlo simulation of the circuit has been done to study the effect of mismatch and temperature variations. The circuits are simulated in TSPICE. Comparison with previous works and between the proposed configurations are also presented.

Keywords: Derivative of Neuron Activation Function, Floating Gate MOSFET, Neuron Activation Function, Sigmoid, Low Power Circuit, Cross Coupled Differential Pair.

I. INTRODUCTION

Analog implementation of neural networks requires circuits which can generate Neuron Activation Function (NAF) and Derivative of Neuron Activation Function (DNAF). The NAF circuits are required to represent individual neurons and the DNAF circuits are needed to realize the
training of the network [1-3]. The transconductance elements using differential pairs are used as the building block of NAF circuits with sigmoid characteristics [1]-[6]. Application of cross coupled differential pairs improves the linearity of the transconductance elements [7]. The DNAF can be realized based on the definition of approximate derivative of a function [2][5][8]. Ability of adaptation to environment is a major advantage of neural network which demands programmable characteristics for NAF and DNAF [5][7]. While the differential pair can be used to realize NAF function, asymmetry in the differential pair in the form of asymmetry in the area of the devices [10] or offset voltage [3][5] or back gate effect can be used to realize DNAF [11].

Due to the charge retention property and adjustable threshold voltage, Floating Gate MOSFET (FGMOSFET) has been used for analog signal processing applications and also for realizing memories [12]-[16]. FGMOSFET is also suitable for low voltage applications as its threshold voltage can be reduced by increasing the bias voltage applied to one of the control gates [17]. It has the additional advantage of wide linear range due to the internal voltage division [18]. Two novel circuit techniques are presented in this paper. The first circuit uses standard CMOS differential pair to realize NAF and transistor asymmetry is used to realize DNAF. The characteristics such as slope and threshold levels of NAF and scaling factor of the derivative can be continuously programmed.

In the second circuit advantages of FGMOSFET devices are exploited to realize low voltage NAF/DNAF circuit with wide linear range. FGMOS differential pair is used to realize NAF and DNAF is generated by introducing asymmetry in threshold voltages between the cross coupled FGMOS differential pairs’ which is effected by difference in bias voltages applied to one of the control gates of FGMOS differential pairs. This circuit generates log sigmoid and tan sigmoid NAF functions and their derivative function (DNAF) simultaneously, with external programmability of the characteristics of these functions. The programmability is achieved by the use of one of the control gates of FGMOSFET. The characteristics of the NAF and DNAF function can be continuously programmed by applying external control voltages.

Many applications using neural networks require programmable characteristics of NAF and DNAF [5] [9]. The proposed circuits can generate both programmable NAF and DNAF.

II. PRINCIPLE OF NAF AND DNAF

The behavior of neuron activation function can be represented by a log sigmoid function or a tan sigmoid function given by (1) and (2) respectively [5].

\[ f(x) = \frac{1}{1 + e^{-\lambda(x+\alpha)}} \quad (1) \]

\[ Y = \tanh(\lambda(x+\alpha)) \quad (2) \]

where \( \lambda \) is the slope parameter and \( \alpha \) the threshold parameter. Log sigmoid function is unipolar and tan sigmoid is bipolar (fig.1 (a)). It may be noted that log sigmoid function can be obtained by adding a dc to tan sigmoid function.

In neural networks NAF with varying slope and varying threshold levels are required as in fig.1 for learning and evaluation [5],[9].

During the learning phase, the DNAF is required to change the weight of synapses adaptively [3]-[4]. The approximate derivative of a function \( f(x) \) is obtained by the principle of difference approximation [3] as given by (3).
\[ f'(x) = \frac{f(x + \Delta x) - f(x)}{\Delta x} \]  

Circuit realization of the derivative can be obtained by taking the difference of currents of two differential pairs, where \( \Delta x \) in (3) corresponds to a small difference in bias voltage effected by external reference voltage or asymmetry in the devices [3]-[5], [6] [8].

![Fig.1: Plots of Neuron Activation Functions](image)

(a) log sigmoid and tan sigmoid functions (b) log sigmoid with \( \alpha = 0 \) and varying \( \lambda \) (c) log sigmoid with constant \( \lambda \) and varying \( \alpha \)

A. CMOS Based NAF –DNAF Circuit

The proposed circuit of NAF/DNAF is shown in Fig.2 which consists of two differential pairs, one formed by \( M_1, M_2 \) and the other by \( M_3, M_4 \). This circuit generates both tan sigmoid and log sigmoid neuron activation functions depending on the value of \( V_3 \). Using this circuit, NAF with continuously varying slope and threshold levels can be generated. DNAF is realized by creating an asymmetry between the two differential pairs. In this circuit, asymmetry is introduced in the dimensions of the MOSFETs (W/L) forming the two differential pairs. The currents in the transistors of the differential pairs, \( I_{M1}, I_{M2}, I_{M3} \) and \( I_{M4} \) are given by (4)-(7).

\[
I_{M1} = \frac{I_s}{2} + \frac{\beta}{2} V_d \sqrt{\frac{I_s}{\beta} - \frac{V_d^2}{4}}
\]

\[
I_{M2} = \frac{I_s}{2} - \frac{\beta}{2} V_d \sqrt{\frac{I_s}{\beta} - \frac{V_d^2}{4}}
\]

\[
I_{M3} = \frac{I_s}{1 + k} \cdot \frac{k\beta}{1 + k} V_d \sqrt{\frac{2I_s}{(1 + k)\beta} - \frac{kV_d^2}{(1 + k)^2} + \frac{k(k - 1)V_d^2}{(1 + k)^2}}
\]
\[ I_{M3} = \frac{kI_d}{1+k} - \frac{k\beta V}{1+k} \sqrt{\frac{2I_d}{(1+k)\beta} - \frac{kV_p^2}{(1+k)^2} - \frac{k(k-1)V_p^2}{(1+k)^2}} \]  

(7)

\( k \) in (6) and (7) represents the ratio of transconductance parameters of \( M_3 \) and \( M_4 \).

In fig. 2, \( V_{OUT1} \) represents log sigmoid NAF given by (4) and tan sigmoid NAF given by (10) according to the value of \( V_3 \). When \( V_3 = 0V \) the transistor \( M_{11} \) conducts and we get tan sigmoid function. When \( V_3 = -1V \) \( M_{11} \) is in cut off region and we get log sigmoid function. Equation (13) shows that \( V_{OUT1} - V_{OUT2} \) represents the approximate derivative of \( V_{OUT1} \) by the difference approximation i.e., \( V_{OUT1} - V_{OUT2} \) represents the Derivative of Neuron Activation Function.

![Diagram of Proposed NAF/DNAF circuit](image)

where, \( \Delta I \) is the difference in drain currents of the differential pairs due to asymmetry of the MOS transistors.

\[ I_{M5} - I_{M7} = \Delta I \]  

(12)

\[ . \quad V_{OUT1} - V_{OUT2} = \Delta I \cdot R \]  

(13)

In fig. 2 \( V_{OUT1} \) represents log sigmoid NAF given by (4) and tan sigmoid NAF given by (10) according to the value of \( V_3 \). When \( V_3 = 0V \) the transistor \( M_{11} \) conducts and we get tan sigmoid function. When \( V_3 = -1V \) \( M_{11} \) is in cut off region and we get log sigmoid function. Equation (13) shows that \( V_{OUT1} - V_{OUT2} \) represents the approximate derivative of \( V_{OUT1} \) by the difference approximation i.e., \( V_{OUT1} - V_{OUT2} \) represents the Derivative of Neuron Activation Function.
mismatch between the pairs. In the present work, this mismatch is introduced by a difference in transconductance parameters between the transistors of one differential pair.

This introduces a difference in the currents through the differential pairs. Hence $V_{OUT1} - V_{OUT2}$ generates DNAF function as described by (8)-(13). The scaling factor of the DNAF can be varied by varying the resistance values of $M_{12}$ and $M_{13}$. This is achieved by varying the bias voltages at the gate.

**B. Results**

The simulation is done in T-SPICE. The proposed NAF/DNAF circuit generates log sigmoid and tan sigmoid neuron activation functions and their derivative function. Log sigmoid and tan sigmoid function is achieved by setting $V_3$ as -1V or 0V. Fig. 3 shows the simulated outputs at $V_{OUT1}$ which represent log sigmoid and tan sigmoid functions respectively. The solid line represents log sigmoid function and dotted line represent the tan sigmoid function.

**Fig.3:** Neuron Activation Function generated by the proposed NAF/DNAF circuit, dotted line is corresponds to tan sigmoid NAF $I_{OUT1}$ and solid line is corresponds to log sigmoid NAF $I_{OUT1}'$.

**Fig.4a:** Tan sigmoid Neuron Activation Function generated by the proposed NAF/DNAF circuit with varying slope. (b) Log sigmoid Neuron Activation Function generated by the proposed NAF/DNAF circuit with varying slope.

Fig 4(a) and 4(b) shows the tan sigmoid and log sigmoid output of the proposed circuit with varying slopes. The slope of these functions increases with increase in the bias voltage $V_1$ at gate of $M_{12}$ and $M_{13}$. Fig. 5 shows DNAF generated by the proposed circuit.
Fig.5: Derivative of Neuron Activation Function generated by the proposed NAF/DNAF circuit with varying slope

Fig.6 shows the NAF output with varying threshold levels and the corresponding derivatives. If the bias voltage $V_2$ of the MOSFET $M_4$ and $M_2$ increases, the NAF function shift towards the left and shift towards the right as bias voltage decrease. The corresponding curves are shown in Fig.6 (a). Fig.6 (b) represents the derivatives of the shifted NAF function in Fig. 6 (a).

Fig.6: The output of proposed NAF/DNAF circuit (a) The NAF output with varying bias, resulting in a shift of threshold levels. (b) Corresponding DNAF output

Fig.7 shows layout of the proposed CMOS based NAF and DNAF circuit generated using Tanner L Edit.

Fig.7: Layout of proposed NAF/DNAF circuit

Fig.8 shows temperature variation of the proposed CMOS based NAF and DNAF circuit. Temperature is varied from $10^0$ to $60^0$ with an increment of $10^0$. 
C. Comparison with Previous Work

The NAF/DNAF circuit reported in [8] requires an on-chip reference voltage and its power consumption is high. Input to this circuit is a current. The proposed circuit has voltage as input. The circuit in [8] generates only log sigmoid and its derivatives whereas the proposed circuit in this section of the paper generates tan sigmoid and log sigmoid activation functions and their derivative functions with wide range of programmability. The circuit has higher programmability and lower power consumption when compared to [10] and [11].

III. FGMOSFET BASED CIRCUIT FOR NAF AND DNAF

The proposed circuit of NAF/DNAF is shown in Fig.4 which consists of two cross coupled FGMOSFET differential pairs, one formed by $F_{11}$, $F_{12}$ and the other by $F_{21}$ and $F_{22}$. One differential pair is sufficient to generate NAF function. Using this circuit log sigmoid and tan sigmoid NAF with varying slope and threshold levels and the corresponding derivative can be generated simultaneously.

FGMOSFET works on the principle of charge retention by floating gate and addition of signals applied to the control gates [12] [17]. The layout of FGMOSFET used in the present work, its equivalent circuit and circuit symbol are shown in fig. 9.

The threshold voltage of the FGMOSFET is given by (14) [17].

$$V_{th} = V_{th0} + \frac{C_2}{C_1}(V_{bias} - V_{bias})$$

(14)

where,

- $V_{bias}$ voltage applied to control gate 2.
- $V_{th0}$ threshold voltage with zero bias voltage.
- $V_{th}$ threshold voltage with $V_{bias}$ applied to control gate 2.
- $C_1$ capacitance of control gate 1 to floating gate.
- $C_2$ capacitance of control gate 2 to floating gate.

Equation (14) shows that the threshold voltage of FGMOSFET can be continuously varied by varying the voltage at control gate 2 and it is linear function of control gate voltage. The variation in threshold voltage with respect to the bias voltage is shown in fig.10. Hence, in the present work, one of the control gates is proposed to be used for biasing (to fix threshold voltage) and the other as the input. The threshold voltage of the FGMOSFET in terms of the bias voltage is expressed by (15) [17].
\[ V_{th} = V_{th0} - \frac{C_2}{C_1} (V_{bias} + V_{DSS}) \]  

(15)

\[ I_{D11} = \frac{I_m}{2} \left[ 1 + \beta \left( \frac{V_m - \Delta V_{th}}{I_{SS}} \right)^2 - \frac{\beta^2 (V_m - \Delta V_{th})^4}{4I_{SS}^2} \right] \]  

(16)

\[ I_{D12} = \frac{I_m}{2} \left[ 1 - \beta \left( \frac{V_m - \Delta V_{th}}{I_{SS}} \right)^2 + \frac{\beta^2 (V_m - \Delta V_{th})^4}{4I_{SS}^2} \right] \]  

(17)

where \( \beta = \frac{\mu t C_{ox} W}{2L} \)

Also,

\[ I_{OUT1} = I_{D11} \]  

(18)

and

\[ I_{OUT2} = I_{OUT1} I_{SS} \]  

(19)
In (16), (17) $\beta$ represents the transconductance parameter of FGMOSFET, $V_{in}$ represents differential input to differential pair $F_{11}$ and $F_{12}$ and $\Delta V_{th}$ the difference in threshold voltages between them.

In Fig.11 $I_{OUT1}$ equals the current through one of the differential pairs by the current mirror action and represents log sigmoid NAF as given by (16) and (18). $I_{OUT2}$ represents tan sigmoid NAF by subtracting a dc current from log sigmoid function as given by (19). The NAF characteristics can be shifted to left or right by reducing the threshold voltage of $F_{11}$ or $F_{12}$ respectively keeping the other constant. This can be done in the circuit by increasing $V_{BIAS11}$ or $V_{BIAS12}$ keeping the other constant. The curves shift right when $V_{BIAS12}$ is increased, keeping $V_{BIAS11}$ constant. If $V_{BIAS11} = V_{BIAS12}$ transconductance curve without any shift is obtained.

In this work DNAF is realized by creating an asymmetry between the two cross coupled differential pairs. Asymmetry is introduced by creating a mismatch in the threshold voltages of FGMOSFETs forming the two differential pairs. The threshold voltages of the FGMOSFETs can be varied by changing the bias voltage applied to one of the control gates. The currents in the second differential pairs formed by $F_{21}$ and $F_{22}$, $I_{D21}$ and $I_{D22}$ are given by (20)-(21).

$$I_{D21} = \frac{I_o}{2} \left[ 1 + \frac{\beta(V_o - \Delta V_{th2})^2 - \beta^2(V_o - \Delta V_{th3})^4}{4I_{SS}^2} \right]$$  
$$I_{D22} = \frac{I_o}{2} \left[ 1 - \frac{\beta(V_o - \Delta V_{th2})^2 - \beta^2(V_o - \Delta V_{th3})^4}{4I_{SS}^2} \right]$$  

$\Delta V_{TH2}$ in (20) and (21) represents the difference in threshold voltages of transistors in the second differential pair formed by $F_{21}$, $F_{22}$.

The principle of the proposed circuit in generating DNAF is as explained below.

From Fig.4,

$$I_{OUT3} = I_{D21} + I_{D22} - I_{SS} \quad (22)$$

and,

$$I_{D21} + I_{D22} = I_{SS} \quad (23)$$

Let the difference in drain currents of the differential pairs due to the difference in threshold voltages of the FGMOSFET transistors be $\Delta I$.

$$I_{D21} - I_{D21} = \Delta I \quad (24)$$

$$\therefore \ I_{D21} = I_{D21} + \Delta I = I_{OUT2} + \frac{I_{SS}}{2} + \Delta I \quad (25)$$

$$\therefore \ I_{OUT3} = I_{D21} - I_{D21} = (I_{OUT2} + \frac{I_{SS}}{2} + \Delta I) - (I_{OUT2} + \frac{I_{SS}}{2})$$

$$= (I_{OUT2} + \Delta I) - I_{OUT2} \quad (26)$$
In Fig. 11, $I_{OUT1}$, $I_{OUT2}$ represents log sigmoid NAF as given by (16) and (18) and $I_{OUT3}$ represents tan sigmoid NAF as given by (19). Equation (26) shows that $I_{OUT3}$ represents the approximate derivative of $I_{OUT2}$ by the difference approximation i.e., $I_{OUT3}$ represents the Derivative of Neuron Activation Function. For the same NAF, derivatives with varying scaling factors can be generated by changing $\Delta I$. In this circuit it is done by varying the relative bias voltages at the control gates of FGMOSFETs.

The slope ($\lambda$) of the NAF function can be increased by increasing bias voltage applied to the two differential pairs simultaneously. The threshold levels ($\alpha$) of the NAF function can be shifted to left or right by reducing the threshold voltage of $F_{11}$ or $F_{12}$ respectively by keeping the other constant as is evident from (16) and (17). This can be done by increasing bias of $F_{11}$ or $F_{12}$ respectively by keeping the other constant.

By the principle of difference approximation, DNAF can be obtained as the difference of currents in the two cross coupled differential pairs. The difference in currents can be introduced by creating a mismatch between the pairs. In the present work, this mismatch is introduced by a difference in threshold voltages between the transistors of two differential pairs. This is done by changing the relative values of bias voltages applied to the differential pairs. This introduces a difference in the currents through the differential pairs. Hence $I_{OUT3}$ represents DNAF function as described by (22)-(26). The scaling factor of the DNAF can be varied by varying the difference in currents between the two differential pairs. This is achieved by varying the difference in bias voltages between the differential pairs.

### A. Results

The simulation is done in TSPICE with 2$\mu$m CMOS technology. The proposed NAF/DNAF circuit generates log sigmoid and tan sigmoid neuron activation functions and their derivative function simultaneously at $I_{OUT1}$, $I_{OUT2}$ and $I_{OUT3}$ respectively of Fig. 11. Fig. 12 shows the simulated outputs $I_{OUT1}$ and $I_{OUT2}$ which represent log sigmoid and tan sigmoid functions respectively. The solid line represents log sigmoid function and dotted line represent the tan sigmoid function.
**Fig. 12:** Neuron Activation Function generated by FGMOS based NAF/DNAF circuit. Dotted line corresponds to tan sigmoid NAF $I_{OUT1}$ and solid line corresponds to log sigmoid NAF $I_{OUT1}$

Fig. 13 shows the simulated outputs of standard CMOS based NAF/DNAF circuit [9] and proposed FGMOSFET circuit for the same supply voltage. It can be noticed that the linear range of FGMOSFET based circuit is ±1.2V whereas that of the CMOS circuit is only ±0.4V.

**Fig. 13:** Neuron Activation Function and its derivative (a) NAF/ DNAF output from standard CMOS circuit. (b). NAF/ DNAF output from the proposed FGMOSFET circuit

Fig 14 shows the log sigmoid output of the proposed circuit with varying slopes. The slope of these functions increases with increase in the bias voltages $V_{bias11}$ and $V_{bias12}$ of the differential pair formed by $F_{11}$ and $F_{12}$.

**Fig. 14:** Neuron Activation Function generated by FGMOS based NAF/DNAF circuit with varying slope

Fig. 15 shows the NAF output with varying threshold levels and the corresponding derivatives. If the bias voltage of the FGMOSFET $F_{11}$ increases with respect to bias voltage of
FGMOSFET F\textsubscript{12}, the NAF function shift towards the left and if bias voltage of the FGMOSFET F\textsubscript{12} increase with respect to bias voltage of FGMOSFET F\textsubscript{11}, the NAF function shift towards the right. The corresponding curves are shown in fig.15(a). Fig.15(b) represents the derivatives of the shifted NAF function in fig. 15(a).

![Image](image1.png)

Fig.15: The output of proposed NAF/DNAF circuit with a supply voltage of 1.5V. (a) The NAF output with varying bias, resulting in a shift of threshold levels. (b) Corresponding DNAF output

Fig.16 shows the shift in NAF curve with respect to the change in bias voltage of the differential pair transistors F\textsubscript{11} and F\textsubscript{12}. The shift in threshold levels changes linearly with change in bias voltage. This plot shows that when change in bias voltage is positive shift is towards right and if it is negative shift is towards left. If there is no change in bias voltage, shift is zero.

![Image](image2.png)

Fig.16: Change in bias voltage versus shift in NAF curve (shift in threshold levels)

Fig. 17 shows DNAF function with different scaling factors for the same NAF function. This is generated by keeping the bias voltages of the first differential pair equal and constant and keeping the bias voltages of the second differential pair equal and increasing this with respect to the first differential pair.
Fig. 17: Scaled derivatives of Neuron Activation Function obtained with $V_{\text{bias11}} = V_{\text{bias12}}$ and increasing $V_{\text{bias21}} = V_{\text{bias22}}$.

Layout of the proposed floating gate based NAF/DNAF circuit generated using TSPICE is shown in Fig. 18.

Fig. 18: Layout of the floating gate based NAF/DNAF circuit

This is achieved by varying the difference in bias voltages between the differential pairs.

IV. EFFECT OF DEVICE MISMATCH USING MONTE-CARLO ANALYSIS

Mismatch represents the variation in one component value with respect to variation in another component value in a symmetric circuit. Matching property greatly influences analog circuit design. Major sources of device mismatch include threshold voltage mismatch, W-L mismatch and mismatch in the input capacitances. Monte Carlo simulation of the proposed FGMOSFET circuit has been done to estimate the effect of mismatch and temperature variations.

A. Mismatch in the Threshold Voltage of the Input Transistors

One of the drawbacks of the FGMOS devices is that any variation in the threshold voltage of the MOS transistor used to build the FGMOS is equivalent to $C_T/C_{\text{IN}}$ multiplied by the variation at the equivalent input. As the term $C_T/C_{\text{IN}}$ is always greater than one, the effects of the equivalent variation are always going to be greater than the effects it has in a normal MOS device.

\[
V_o = \frac{C_T}{C_{\text{IN}}} \Delta V_{TH} = \frac{C_T}{C_{\text{IN}}} (V_{TH2} - V_{TH1})
\]

\[
\Delta V_{\text{eff,in}} = (V_{\text{in}}^+ - V_{\text{in}}^-) + \frac{C_T}{C_{\text{IN}}} (V_{TH2} - V_{TH1})
\]
\[ \Delta V_{in}^{\text{effective}} = (V_{in}^+ - V_{in}^-) + V_o \quad (29) \]

Monte-Carlo simulation is done to estimate the effect of mismatch in threshold voltage of n-type FGMOS differential amplifier. Threshold voltage of the FGMOS differential pairs using NMOS is taken from uniform distribution centered at 0.622490 for \( F_1 \) and \( F_2 \) with relative variation of 1% for \( F_1 \) and \( F_2 \).

**B. Mismatch in the Channel Width(W) and Channel length(L)**

The matching performance is related not only to the gate area, but also individually to the effective channel length \( L \) and width \( W \). Hence, for a given area \( WL \), the mismatch is significantly altered by varying the aspect ratio \( W/L \).

\[ Area_{FG} = Area_{dmos} + Area_{asymmetricpair} \quad (30) \]

\[ \sigma_{due\ to\ WL} = \frac{A_p}{\sqrt{W/L}} \quad (31) \]

where \( \sigma \) is the standard deviation, \( A_p \) the aspect ratio \( W \) the channel width length, and \( L \) channel length. Lower the standard deviation \( (\sigma) \) better the matching performance of the circuit.

**V. COMPARISON WITH PREVIOUS WORK**

The NAF/DNAF reported in [10] has a linear range of ±0.4V where as the proposed circuit has a much wider linear range of ±1.2V with same supply voltage. The proposed circuit generates log sigmoid and tan sigmoid NAF and their derivative functions simultaneously without any extra hardware. In the present work slope and threshold levels of NAF can be continuously programmed externally by changing the bias voltages without changing the bias current. In [10] a control voltage is used to switch between NAF and DNAF. Compared to the previous works the proposed circuit has a much wider linear range, better programmability of NAF and DNAF functions and lower power consumption. Monte Carlo simulation results shows that the circuit is not affected by slight mismatch in transistors or temperature variations.

**VI. CONCLUSION**

The analysis and simulation results and the layout of two novel circuits which generates programmable log sigmoid and tan sigmoid Neuron Activation Functions and their Derivative Function (NAF and DNAF) are presented.

The first proposed circuit uses CMOS based differential pairs to obtain neuron activation function and asymmetry in transistors forming differential pairs to obtain DNAF. In this circuit slope and threshold levels of the NAF and the scaling factor of DNAF can be continuously programmed externally by changing the bias voltage at the gate of transistors. The programmability is achieved without any extra hardware. This proposed circuit is simulated in T-SPICE, using transistors model for a standard 90nm CMOS technology with supply voltage \( \pm 200mV \).

The second circuit offers low voltage operation due to low threshold voltage of FGMOSFET and wide linear range due to the internal voltage division in FGMOSFET. This circuit uses FGMOSFET based cross coupled differential pairs. Since the FGMOSFET devices have an extra control gate compared to the MOSFET, external voltage applied at the appropriate devices help to change the characteristics of the NAF and DNAF. In this circuit slope and threshold levels of the...
NAF and the scaling factor of DNAF can be continuously programmed externally by changing the bias voltages. Here also, the programmability is achieved without any extra hardware. As this circuit is based on FGMOSFETs, the NAF has a wide linear range and it is equal to ±1.2V with a power supply of 1.5V, where as the linear range of standard CMOS circuit with same supply voltage is only ±0.4V.

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AUTHOR’S DETAIL

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