MODIFIED TWO PHASE DRIVE ADIABATIC DYNAMIC CMOS LOGIC

Praveer Saxena¹, Swati Dhamani², Dinesh Chandra³, Sampath Kumar V⁴

¹Asst. Professor, Deptt. of ECE, A.I.M.T., Gr. Noida, India.
²Student, M.Tech (VLSI Design), H.C.S.T., Mathura, India.
³Professor & Head, Deptt. of ECE, J.S.S.A.T.E., Noida, India.
⁴Asst. Professor, Deptt. of ECE, J.S.S.A.T.E., Noida, India.

¹praveer82@gmail.com
²dhamaniswati@rediffmail.com
³dinesshc@gmail.com
⁴sampath_sams@yahoo.com

ABSTRACT

As the device dimensions are shrinking accompanied with increased packing density to give rise to more functionality and increased performance, the power dissipation has become a big concern. A promising technique to achieve low power dissipation is adiabatic switching. Several adiabatic approaches have been discussed by authors in the literature. One of the promising adiabatic techniques is 2 phase drive adiabatic dynamic CMOS logic. But 2PADCL suffer from floating output node. The floating node may give rise to erroneous output. In this paper modified 2PADCL has been proposed which eliminates the drawback due to floating output node in conventional 2PADCL.

Keywords: adiabatic, energy recovery, low power, floating node.

1. INTRODUCTION

Low power consumption has become a necessary requirement in today’s world of fast and smaller devices. Several techniques to achieve low power dissipation have been reported [2], [3]. Although static CMOS has been a good choice due to its low power dissipation and small fabrication space, the logic circuits based on static CMOS still consumes significant amount of power. The main source of power dissipation in CMOS is dynamic power [2], [3]. One of the promising techniques to
achieve low power dissipation is adiabatic switching [3]. Logic circuits based on adiabatic logic have been widely reported by authors in the literature [1], [6], [8], [9], [10], [11], [12], [13], [17], [18].

Adiabatic logic is basically a circuit level technique to minimize the dynamic power. It basically works on minimizing the dissipation across the ON resistance of MOSFETs by using slowly varying power clocks and by recovering the part of energy given to the output back to the source so that it can be used again.

Several adiabatic approaches have been proposed by the authors in their literature, each having some advantages and disadvantages [1], [6], [8], [9], [12], [13], [17], [18]. One of the promising adiabatic techniques is 2PADCL [18]. It consumes low power and provides small delay in implementing logic blocks. 2PADCL suffers from floating output node due to alternate hold phases in power clock [8], [18]. Floating output node may give rise to wrong output due to noise coupling or charge leakage etc. In this paper, modified 2PADCL logic is proposed to deal with floating output node problem.

2. PREVIOUS WORK : TWO PHASE DRIVE ADIABATIC DYNAMIC CMOS LOGIC

The 2PADCL family was proposed by Takahashi, Fukuta, Sekine and Yokoyama [18] and is discussed in implementing a 1-bit full adder by Saxena, Chandra and Kumar [10]. It uses two clocks as power supplies with 180° phase difference between them. The supply waveform consists of two modes, “evaluation” and “hold” as shown in Figure 1. When Vclk and \( \overline{Vclk} \) are in evaluate mode, there is conducting path in either PMOS devices or NMOS devices. Output node may evaluate from low to high or from high to low or remain unchanged. When Vclk and \( \overline{Vclk} \) are in hold mode, output node holds its value in spite of the fact that Vclk and \( \overline{Vclk} \) are changing their values. Circuit nodes are not necessarily charging and discharging every clock cycle, reducing the switching activity.

The energy dissipation in this logic family occurs due to threshold voltage of MOSFET, diode cut in potential and energy dissipated in resistance of MOS devices.

The energy dissipation of inverter per stage is

\[
E_{2PADCL} = 2 C_{GS} (V_p - 2V_d) V_d + C_{GS} (V_i - V_d)^2
\]  

(1)

But \( V_i \approx V_d \), as diodes are constructed from MOSFET.

\[
E_{2PADCL} \approx 2C_{GS} (V_p - 2V_d) V_d
\]

(2)

Where \( C_{GS} \) is gate source capacitance of next stage, \( V_p \) is peak value of power clock, \( V_d \) is diode cut-in potential. Here, they have ignored the energy dissipation through ON resistance of MOS devices as this component is very much small in adiabatic logics.

The schematic of 2PADCL inverter and simulation waveform is shown in Figure 1.
3. PROPOSED WORK: MODIFIED TWO PHASE DRIVE ADIABATIC DYNAMIC CMOS LOGIC

In this section, modified two phase drive adiabatic dynamic CMOS is proposed. In modified 2PADCL, 180 degree phase shift between two complementary power clocks is utilized to eliminate the floating node problem. The structure of inverter using modified 2PADCL is shown in Figure 2. Beside the normal 2PADCL inverter structure, it includes two extra diodes shown as M5 and M6.

In M2PADCL, the output node may be charged or discharged by both the power clocks. Initially, if output is logic low and we select the input to be logic low and in case Vclk is rising then the output node will be charged by Vclk through diode (M1) and PMOS (M2). Once Vclk the reaches the peak value and starts decreasing, the output node becomes floating as was the case in 2PADCL. But in modified 2PADCL logic this floating node is soon removed because at the same time the Vclk starts to rise and output node gets connected to Vclk though Diode (M5) and PMOS (M2), hence eliminating the weak HIGH at the output node. Similarly, the weak LOW at the output can be eliminated by path consisting of NMOS (M3) and diode (M6).

The drawback associated with modified 2PADCL over conventional 2PADCL is increased fabrication space due to additional diodes and increased power dissipation due to these diodes. But power dissipation will not be much different from conventional 2PADCL as only one of the charging path or discharging path will be activated at same instant of time.

The schematic of the inverter using modified 2PADCL along with the simulation waveform is shown in Figure 2.
Figure 2: Inverter using modified 2PADCL (M2PADCL) and simulation waveform

If we ignore the energy dissipation in ON resistance of MOSFETs as it is quite low in adiabatic logics, the calculation of energy dissipation of a single inverter implemented with M2PADCL can be given by

$$E_d \approx 2C_L V_{d}(V_p - 2V_d) + 2C_L V_d V_s$$

(3)

Where $V_d$ is the diode cut-in voltage, $C_L$ is the capacitance at the output node consisting of diffusion capacitances of inverter under consideration, wiring capacitance and next stage gate capacitances. $V_s$ is the voltage swing at output node when diode M5 or M6 is conducting. Comparing the equation (3) with equation (2), we can see an extra term for energy dissipation due to diode M5 and M6. As we know these diodes are used to prevent floating output node, the value of $V_s$ depends on change in output due to momentary state of floating output node. In modified 2PADCL, the output node remains floating for very less time, the value of $V_s$ should be very less and energy dissipation due to this should be small.

Other logic structures like NAND, NOR, Full adders can be easily designed with modified two phase drive adiabatic dynamic CMOS logic (M2PADCL) much like with conventional 2PADCL except inclusion of two extra diodes to eliminate floating node. The NAND and NOR gate using modified 2PADCL are shown in Figure 3 and Figure 4 respectively.

Figure 3: NAND gate and its simulation waveform using modified 2PADCL
Figure 4: NOR gate and its simulation waveform using modified 2PADCL

4. RESULTS

The different logic structures using conventional 2PADCL have been widely reported by authors and have been compared with static CMOS structures under different operating conditions or parameters [10], [18]. To observe that how much power modified 2PADCL based structure dissipates, the NAND gate based on Modified 2PADCL is compared with NAND gate based on Static CMOS and conventional 2PADCL.

In this section the NAND gate designed using static CMOS, conventional 2PADCL and Modified 2PADCL are compared in terms of average power consumption for different value of load capacitance. The 180nm technology parameters provided by predictive technology are used at 1.8V. The width and length of all the MOSFETs are kept at 720nm and 180nm respectively. The power clock frequency is selected to be 100MHz. Input frequencies are 25MHz, 12.5MHz respectively for inputs A and B. The operating temperature is 25°C. The load capacitance $C_L$ is varied from 10f farad to 200f farad in steps of 20f farad and the resulting average power consumption is observed. Here we have used HSPICE for the simulation. The result can be observed in Figure 5.

![Figure 5: Variation of Average Power Consumption with Load Capacitance](image-url)
It can be observed that the power dissipation should increase with increase in load capacitance as dynamic power is directly proportional to load capacitance and simulation results confirm that. Power consumption is rising sharply in static CMOS NAND gate with load capacitance. Power dissipation is also rising in 2PADCL but not that sharply as was with static CMOS saving significant amount of power. Maximum of 66% power saving is achieved by 2PADCL in comparison to static cmos based NAND gate at $C_L = 190$ femto farad.

As expected, NAND gate based on Modified 2PADCL consumes little more power than 2PADCL due to presence of two extra diodes. Maximum of 60% power saving is achieved by modified 2PADCL in comparison to static cmos based NAND gate at $C_L = 190$ femto farad.

5. CONCLUSION

Logic circuits based on conventional 2PADCL consumes very less power but suffer from floating output node due to alternate hold phase and may give rise to wrong output. Modified 2PADCL consumes little more power in comparison to conventional 2PADCL but eliminates the problem due to floating output node. Due to elimination of problem due to floating output node and low power consumption, Modified 2PADCL can be a good choice for low power applications but at the expense of increased propagation delay in comparison to static CMOS as adiabatic logic circuits uses slowly varying power clocks.

REFERENCES


