HALF BRIDGE CONVERTER WITH WIDE RANGE ZVS

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ABSTRACT

A modified full bridge converter topology which can attain ZVS over wide load range and the circulating current is fully eliminated. Two half bridge converters combined together to form a full bridge structure and they are operated in phase shifted mode. The converter can perform in a 50% duty cycle which helps to achieve ZVS over wider load range. The converter is able to perform both PWM mode as well as phase shifted mode. The switching frequency of the converter is 100KHz.

Key words: Full Bridge Converter, Dual Half Bridge Converter, ZVS, Phase Shifting

I. INTRODUCTION

Most popular topologies for high power and high density applications in switching converter is a phase shifted full bridge DCDC converter. Phase shifted full bridge is selected because of its capability for Zero Voltage Switching. This configuration is mainly discussed in Texas Instruments application note. In spite of all the advantages, a problem regarding this topology is its circulating current causing losses and ZVS not applicable for light loads.

Many methods have been introduced to added to the converter’s primary side. This helped to extend the soft switching range but the excess energy in the converter lead to higher voltage spikes in the secondary side rectifier diodes. By introducing a clamping circuit this problem is recovered and this captures most of the transient energy in the primary side which is used for soft switching and is recycled back to the converter’s dc input.

For different output voltages different methods can be used to mitigate the conduction losses. Synchronous MOSFETS are used to minimize the conduction losses for low output voltage such as 48V or below. By maintaining Synchronous FETs active we can achieve continuous conduction mode (CCM) and maintain constant duty cycle. The output inductor current of the converter can be negative, positive and zero depending upon the load. In this case at very light loads especially at zero load, negative mitigate this problem. Resonant inductor is energy become so significant that too much energy is cycled back to the primary side resulting in efficiency loss.

When the output rectification devices are diodes it is difficult to extend ZVS range. Different circuits have been introduced to mitigate this problem. A simple auxiliary circuit on the secondary side provides conditions for ZVS [4]. Another method is a passive LC network connecting to the bridge switches. [5,8]. The major problem regarding the full bridge converter is the presence of circulating current which causes substantial power losses. Many methods have been tried to remove this drawback. One method is resonant converters. Resonant converters will remove circulating current but ZVS is not achieved. Another one is Asymmetrical control. This method is also applicable for low power applications.

We all know that open loop half bridge converter is having higher efficiency at higher loads and can achieve ZVS. The problem regarding this concept is that since PWM is fixed the output voltage cannot be regulated. If two such converters is connected together we can achieve all the desired merits including the regulated output voltage. This
preferred topology which is going to be discussed in this paper can achieve can eliminate the circulating current and can achieve ZVS at wider load range.

II. PREFERRED TOPOLOGY

The preferred topology is a phase shifted dual half bridge converter. Two half bridge converters combined together forms the preferred topology half bridge converter with its improved version is having its output is a current doubler filter and its power transformers secondary is centre tapped to its power ground. Since its secondary is centre tapped we can see as the two interleaved forward converter output connected in parallel with 180°phase offset between the outputs. This helps the filter to fully cancel the current ripple. The converter is operating in 50% duty cycle.

By proper design techniques of the transformer especially magnetizing inductance and dead time control of the primary switch the switch’s parasitic capacitance can be fully discharged before the switch is turned on. By this way the converter can maintain the ZVS over wider load range. These type of two converters when combined together to work like a full bridge structure forms our preferred topology.

The topology include two half bridge inverters: leading half bridge and lagging half bridge. One bridge initiates a pulse while the other terminates the pulse. Resonant inductor and two clamping diodes D1 and D2 can be added to the inverter to perform the conventional performance as in the phase shifted full bridge converter. The inductor stores extra energy to extend soft switching range and eliminate the reverse recovery current of the rectifier diodes.

The specialty of this converter is that the power is transferred from primary to secondary side during D and 1-D periods, this important feature says that the continuous flow of power is always there the converter.

III. DESIGN

Power Rating = 1kw
Input Voltage=385v
Output Voltage=48-50v
Switching Frequency=100 kHz
Input output voltage relationship:
\[ V_0 = V_{in} \times \frac{0.5 + \frac{\varphi}{360^\circ}}{n} \]  

(1)

\[ D = 0.5 + \frac{\varphi}{360^\circ} \]  

(2)

IV. SIMULATION RESULT

Fig 2 PSIM model

Fig 3 Leading and Lagging Inverter Output With 0 a Load

Fig 4 Leading and Lagging Inverter Output with 6A load
The simulation is done using PSIM. The PSIM model and the waveforms is shown as follows:

- **Fig 5** Transformers secondary voltages of T1 and T2
- **Fig 6** T1’s primary voltage and current
- **Fig 7** T2’s primary current
- **Fig 8** Q1 and Q2 achieving ZVS
V. CONCLUSION

By using this new topology so many merits have been achieved. The main one is the operation is possible for wide load range, heavy as well as light loads. Circulating current is eliminated and the efficiency is improved to a high rate. In this case we can achieve 100% of time utilization for power transformation as well as all the components have been utilized completely. The individual stresses of the components are highly reduced. This topology is used for many high as well as low power applications.

VI. REFERENCES